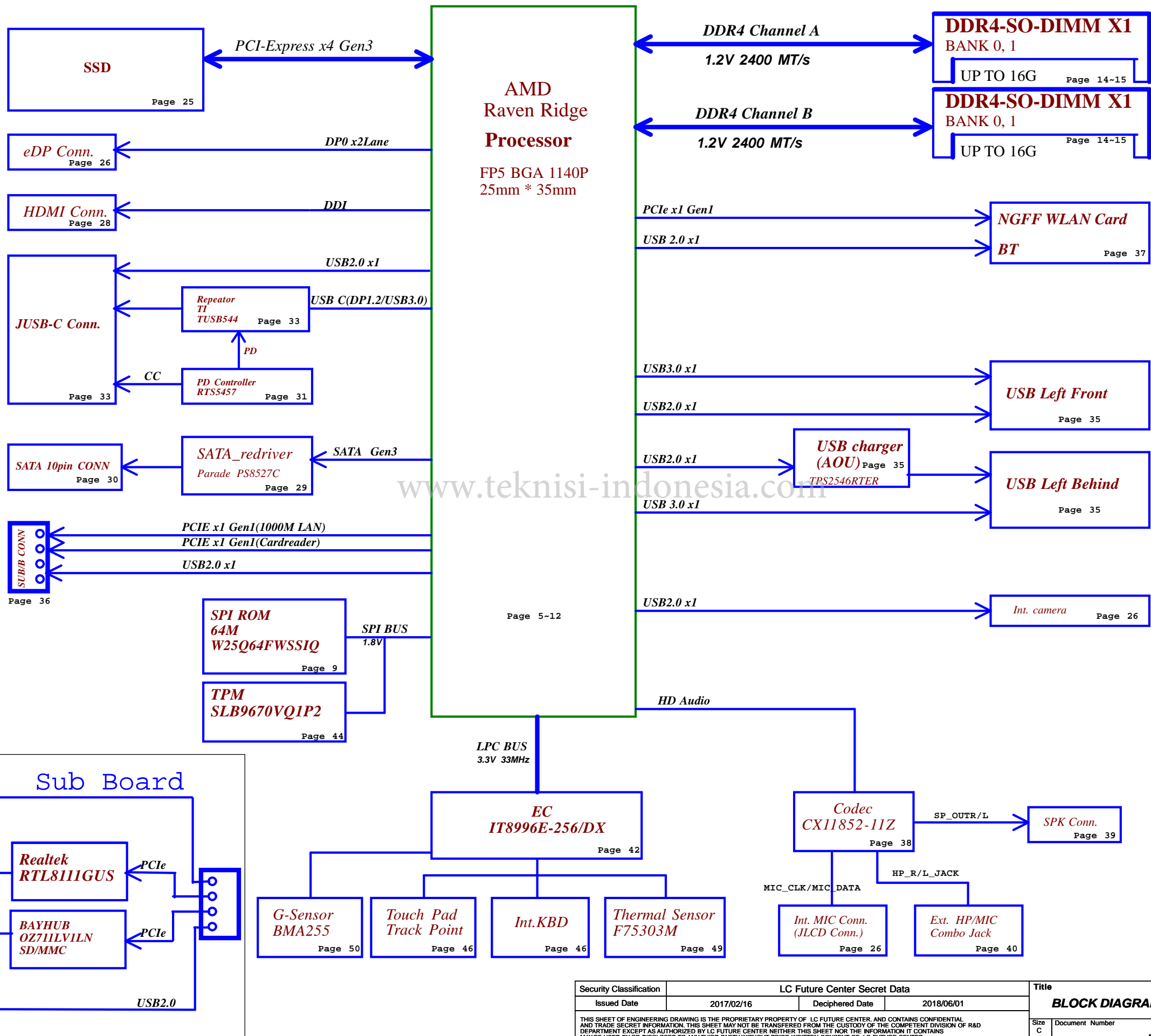


LCFC Confidential
RAVEN EX85 Rev1.0 Schematic

AMD Raven Ridge FP5 Processor with DDR4

2018-04-10 Rev1.0

AMD Raven Ridge FP5



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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane \ State	B9+	+3VALW +5VALW +1.8VALW +0.9VALW_VDDP	+1.2V +2.5V	+5VS +3VS +1.5VS +0.9VS_VDDP +0.6VS +VDDCR_SOC +VDDC_VDD +VGA_CORE +3.3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_A#	SLP_S3#		SLP_S5#	EC_ON	SUSP#
S0	HIGH	HIGH		HIGH	ON	ON
S3 (Suspend to RAM)	LOW	LOW		HIGH	ON	OFF
S4 (Suspend to Disk)	LOW	LOW		HIGH	ON	OFF
S5 (Soft OFF)	LOW	LOW		LOW	ON	OFF

USB2 Port

Port	Device
0	USBC
1	USB3 port1
2	USB3 port2
3	USB2 port1
4	USB2(BT)
5	Int. Camera

USB3 Port

Port	Device
0	USB Type-C
1	USB3 port1
2	USB3 port2
3	USB3 port2
	X
4	X

PCIE Port

Port	Device
GPP0	LAN
GPP1	CardReader
GPP2	X
GPP3	X
GPP4	WLAN
GPP5	X
GFX0	M.2 SSD
GFX1	M.2 SSD
GFX2	M.2 SSD
GFX3	M.2 SSD
GFX4~7	X

SATA Port

Port	Device
1	HDD
2	X

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	APU	CP Module	Charge	PD	G-Sensor	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8996E-256-DX +3VL	X	V +3VL	X	X	X	X	X	V +3VL	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8996E-256-DX +3VALW	X	X	X	X	X	X	X	X	V +3VALW	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8996E-256-DX +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3VS	X	X	X	V +3VS	X
EC_SMB_CK4 EC_SMB_DA4	IT8996E-256-DX +3VL	X	X	X	X	X	X	X	X	X	X	V

APU I2C

APU Port	Net	Device
I2C2_SCL/SDA	APU_SMB0CLK/SDA	DIMM1/DIMM2
I2C3_SCL/SDA	APU_SMB1_CLK/SDA	TOUCHPAD
SIC/SID	EC_SMB_CK3/DA3	Conn EC
USBC_I2C_SCL/SDA	EC_SMB_CK2/DA2	PD

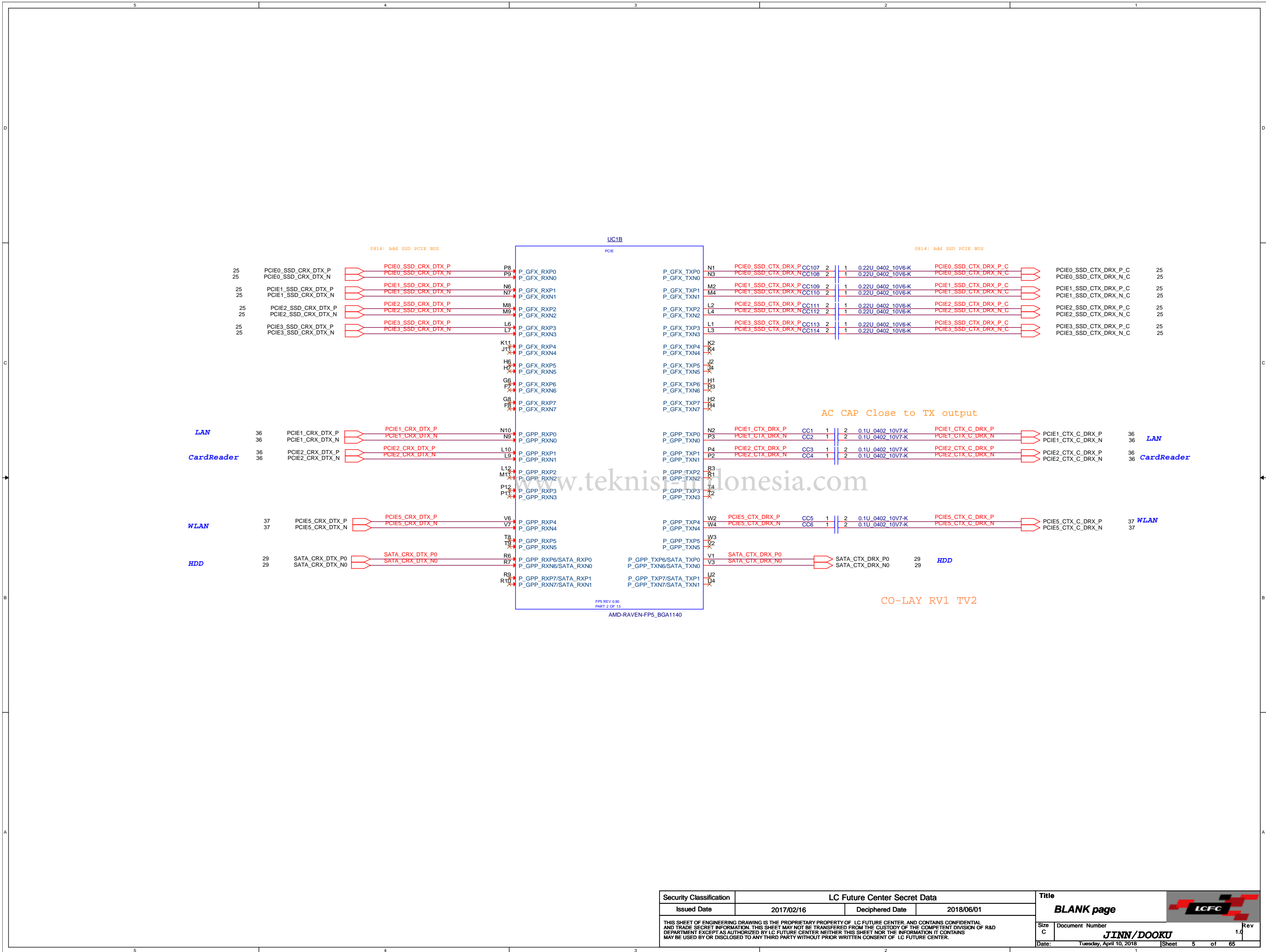
ZZZ2 PCB@
NM-A861
DA800010W0

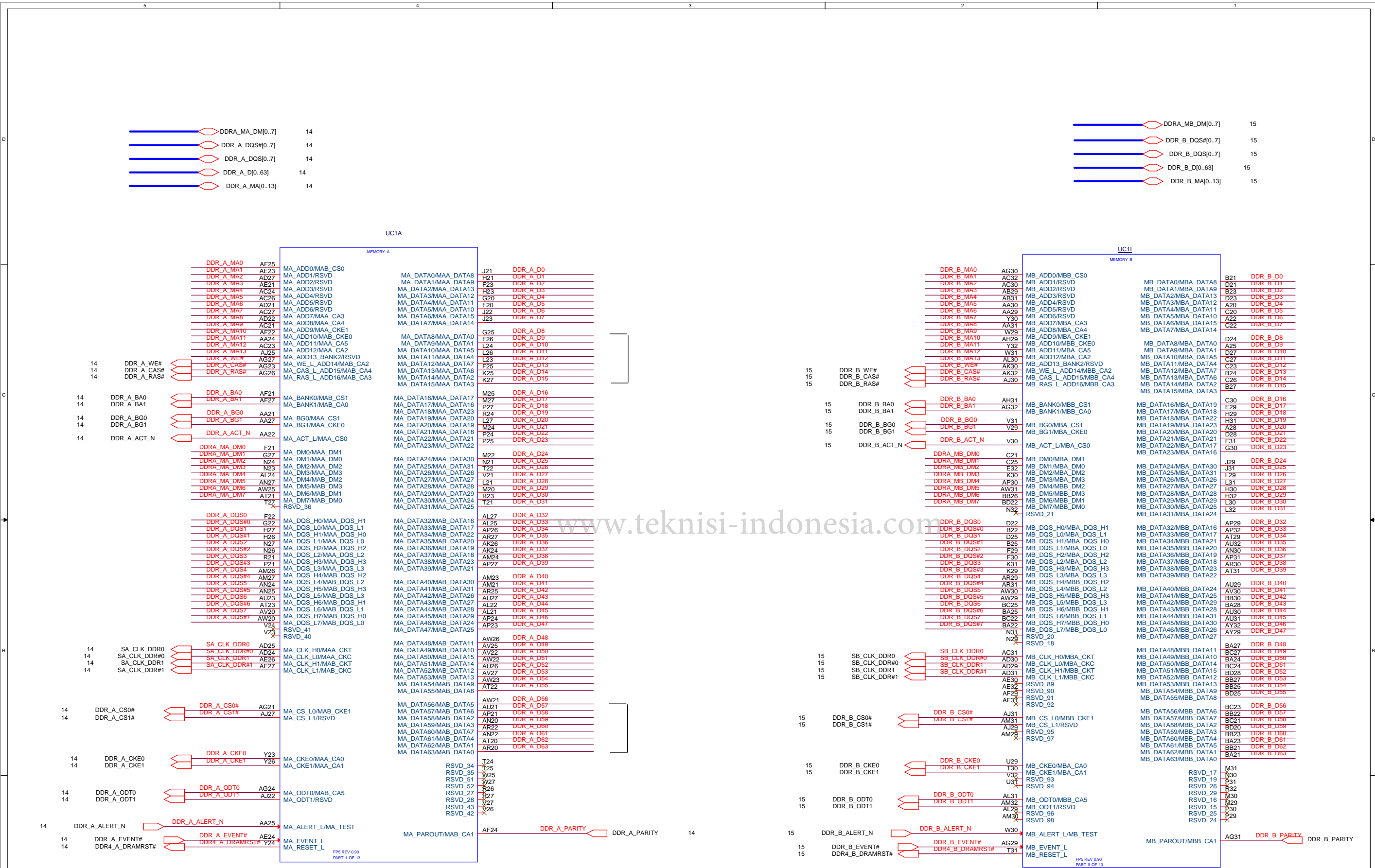
APPLY PCB PN

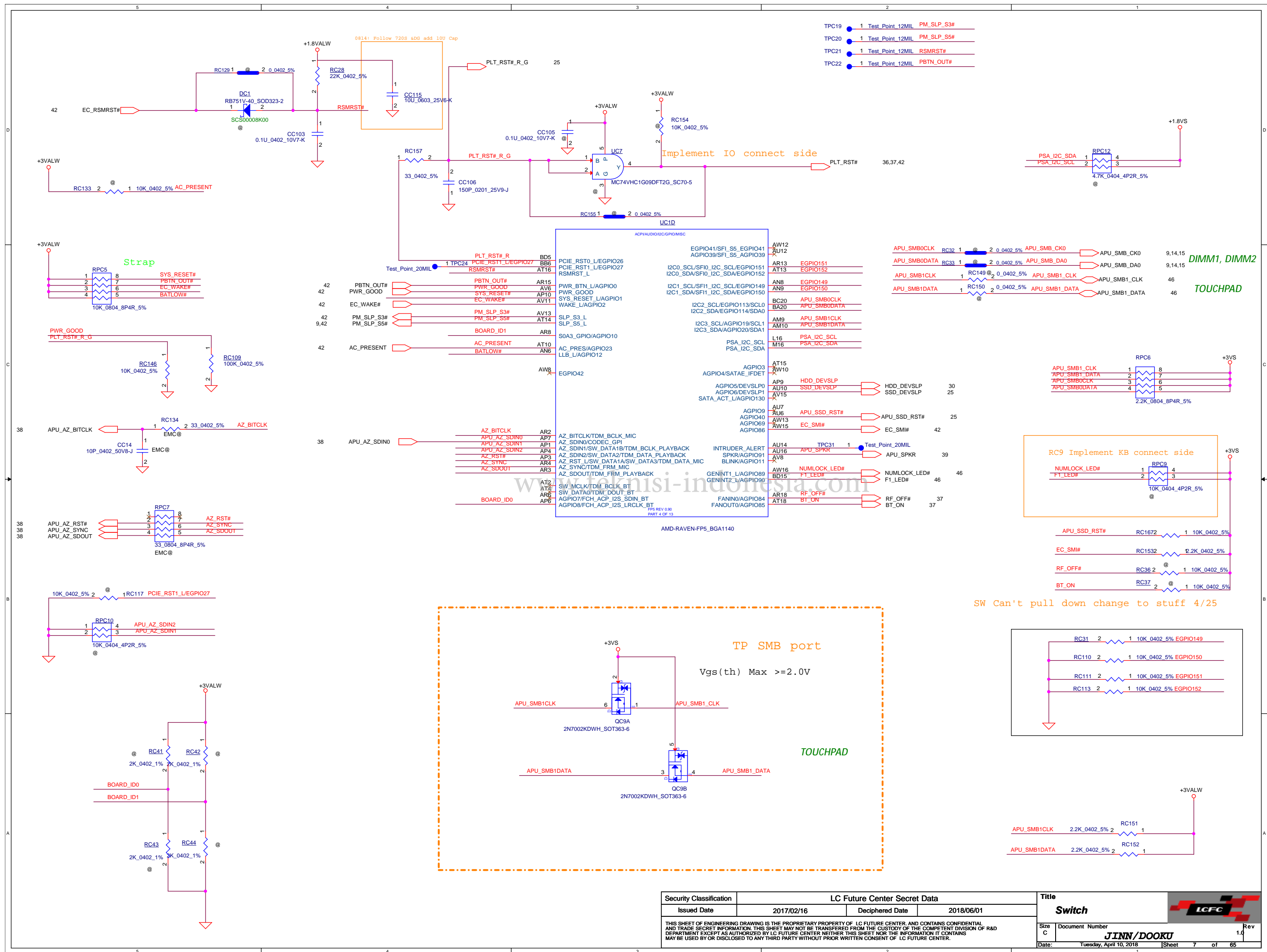
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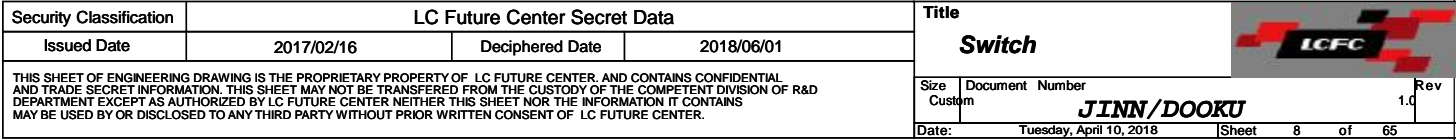
BOM Structure Table

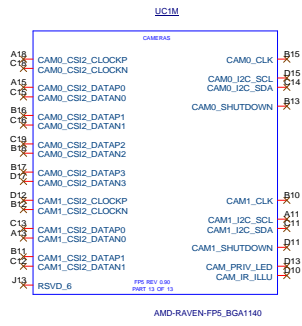
BOM Structure	NOTE
HDT@	For HDT AMD debug port
LPC@	For LPC AMD debug port
TPM@	Trusted Platform Module(TPM)
UMA@	UMA SKU ID
CD@	COST DOWN
EMC_NS@	EMC Reserves
ME@	ME Connector
RF@	For RF function
EMC@	For EMI function
RF_NS@	reserves RF component
RF_PXNS@	VGA reserves RF component



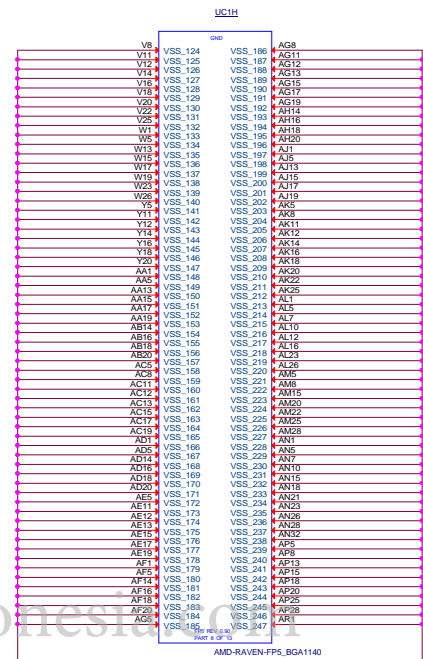
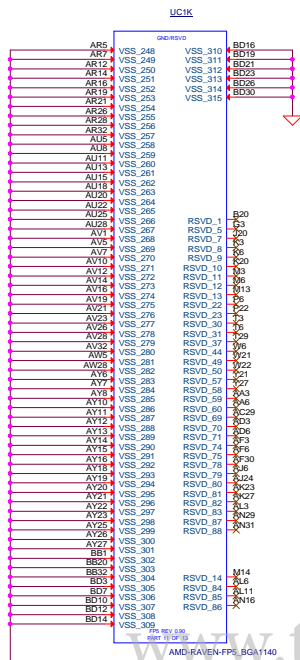
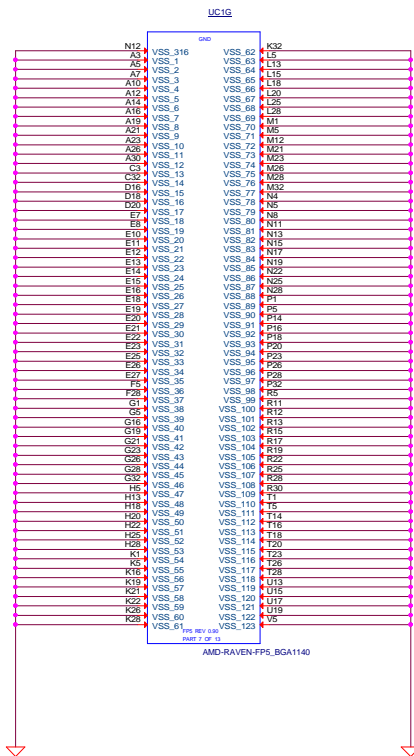


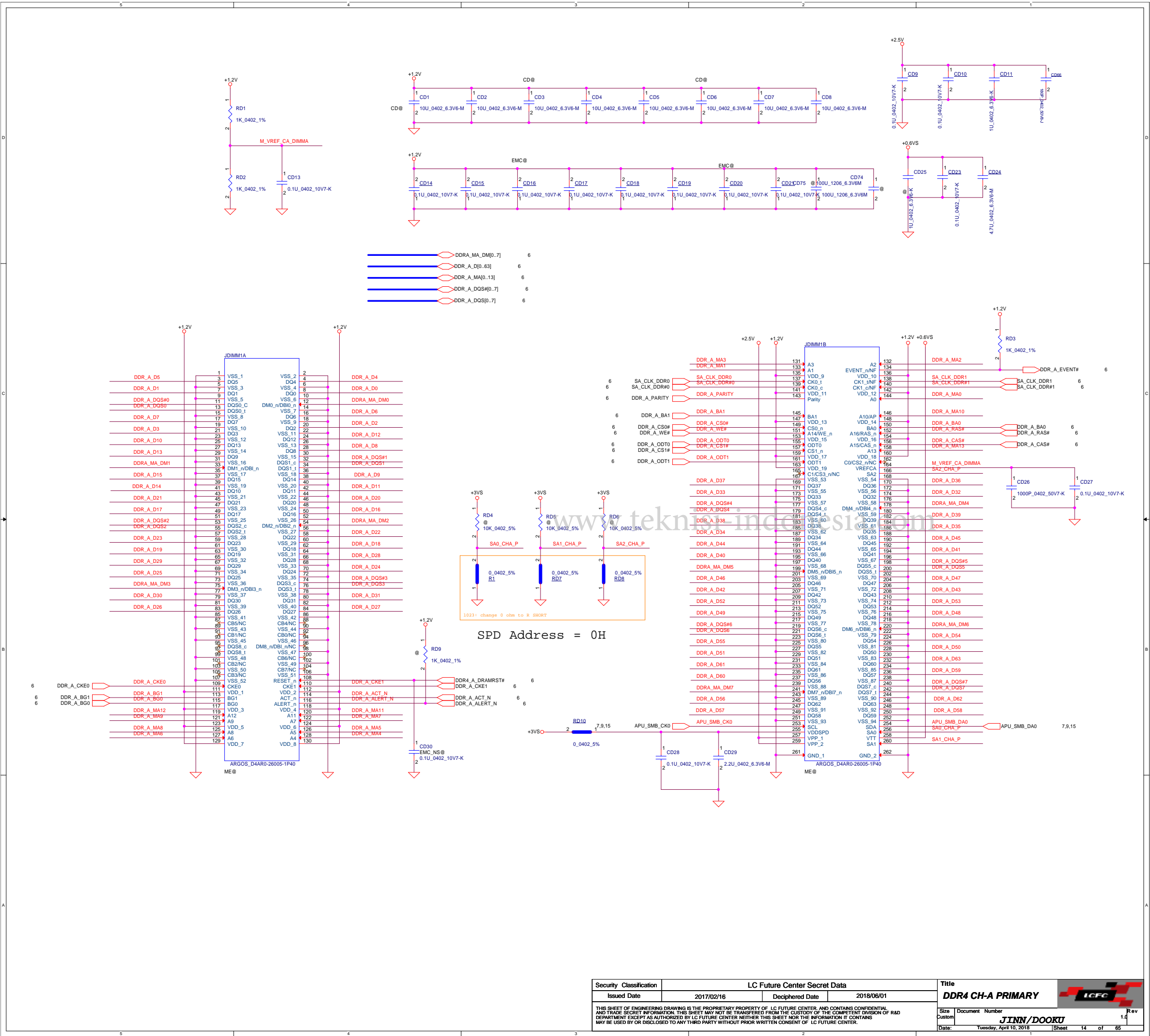


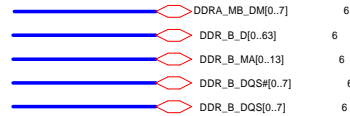
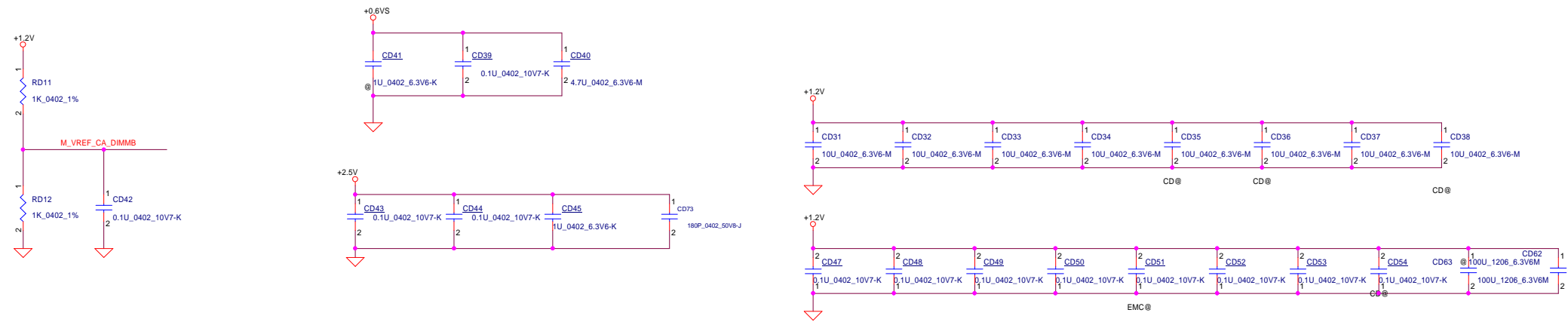




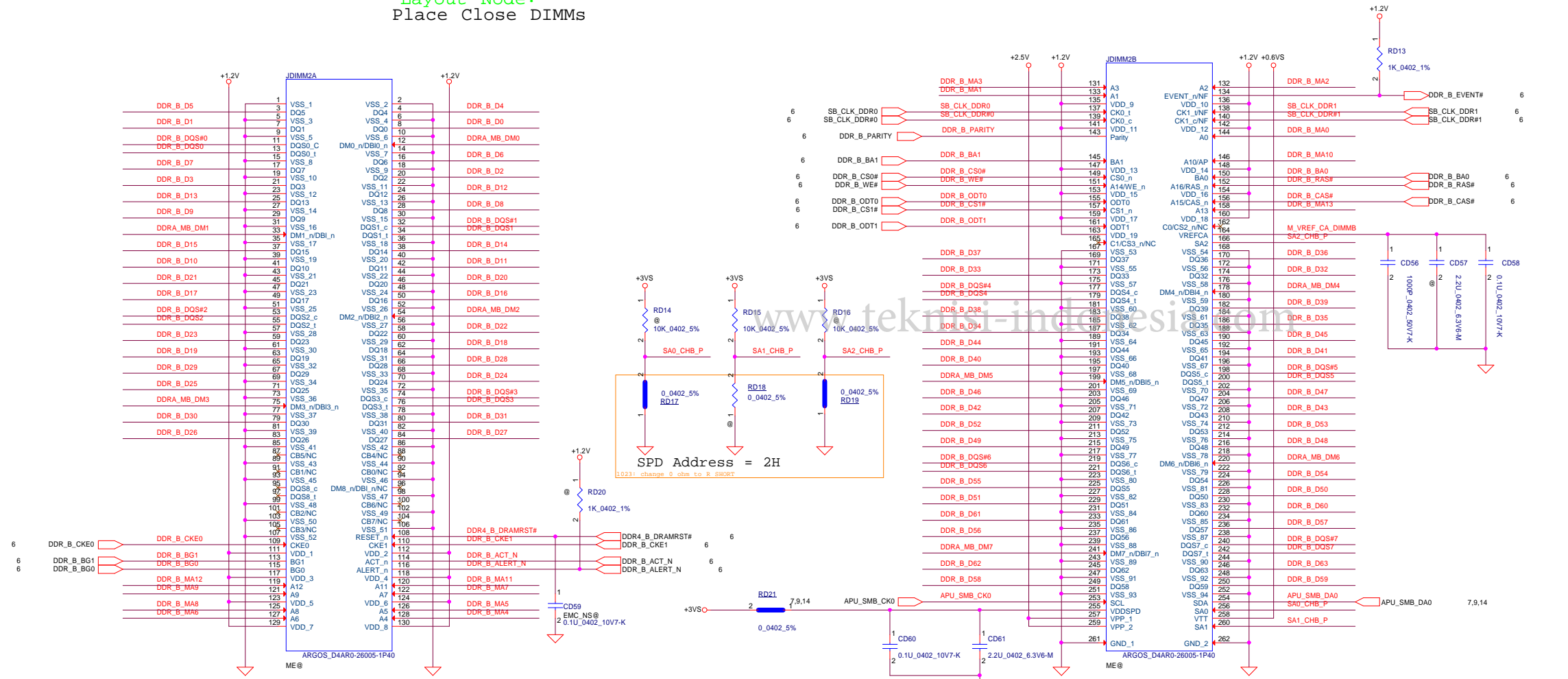
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Layout Node:
Place Close DIMMs



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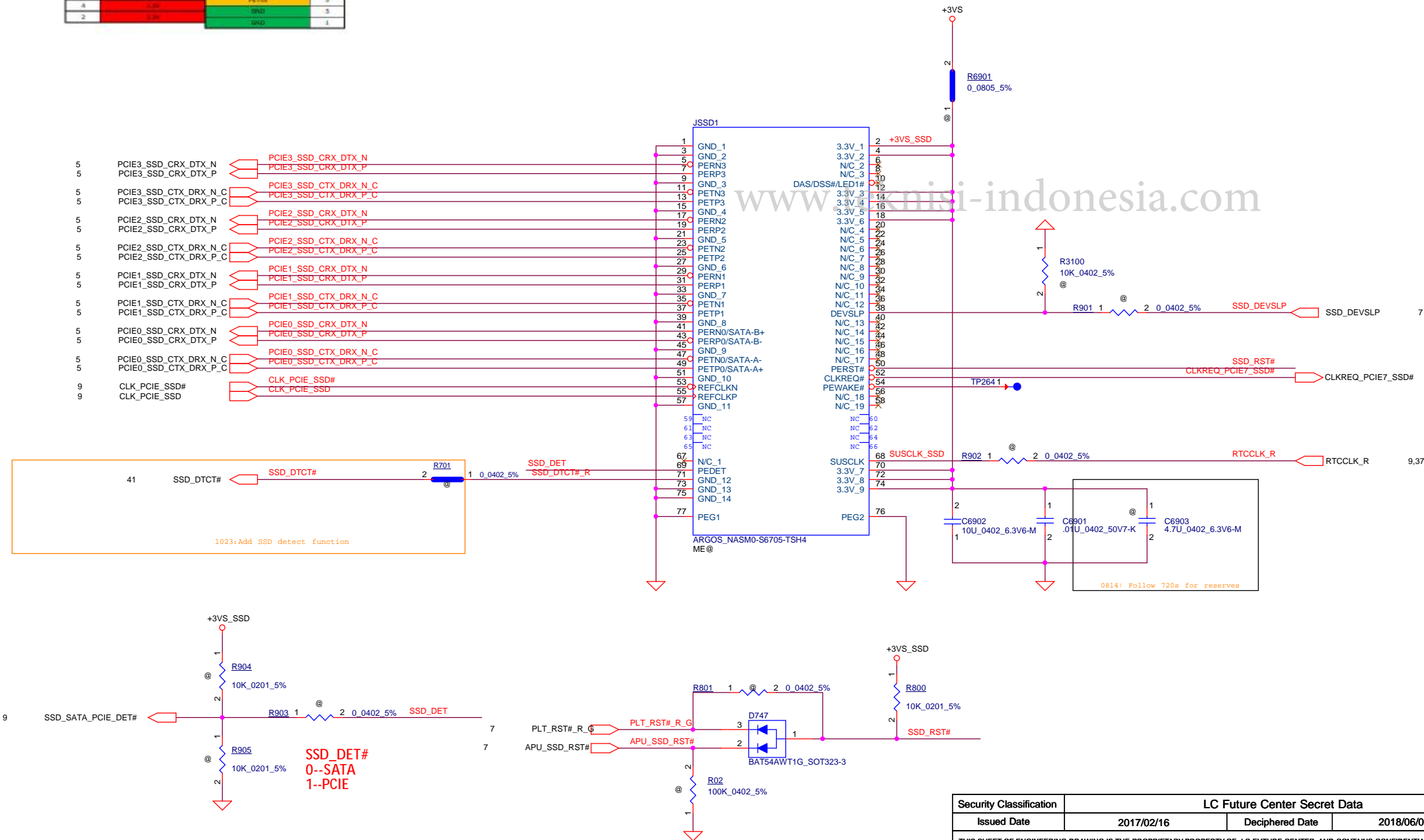
Table 35. Socket 3 PCIe-based Module Pinout

74	3.3V	75	3.3V
72	3.3V	73	3.3V
70	3.3V	71	3.3V
68	SUSCLK (12MHz) (0V/3.3V)	69	PEDET (NC-PCIE)
	Module Key		Module Key
	Module Key		Module Key
	Module Key		Module Key
	Module Key		Module Key
58	Reserved/MFG Clock	57	3.3V
56	Reserved/MFG Data	55	3.3V
54	PERWAKE# (IO)(3.3V)	53	3.3V
52	CLKREQ# (IO)(3.3V)	51	3.3V
50	PERST# (IO)(3.3V)	49	3.3V
48	N/C	47	3.3V
46	N/C	45	3.3V
44	N/C	43	3.3V
42	N/C	41	3.3V
40	N/C	39	3.3V
38	DEVSLP#	37	3.3V
36	N/C	35	3.3V
34	N/C	33	3.3V
32	N/C	31	3.3V
30	N/C	29	3.3V
28	N/C	27	3.3V
26	N/C	25	3.3V
24	N/C	23	3.3V
22	N/C	21	3.3V
20	N/C	19	3.3V
18	N/C	17	3.3V
16	N/C	15	3.3V
14	N/C	13	3.3V
12	N/C	11	3.3V
10	N/C	9	3.3V
8	N/C	7	3.3V
6	N/C	5	3.3V
4	N/C	3	3.3V
2	N/C	1	3.3V

M.2 SSD(M TYPE)

Table 32. Socket 2 PCIe-based SSD Module Pinout

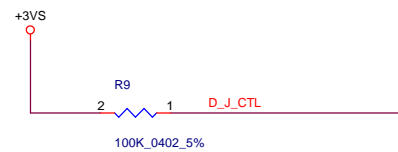
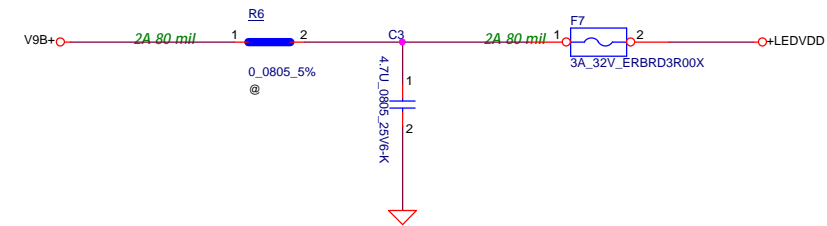
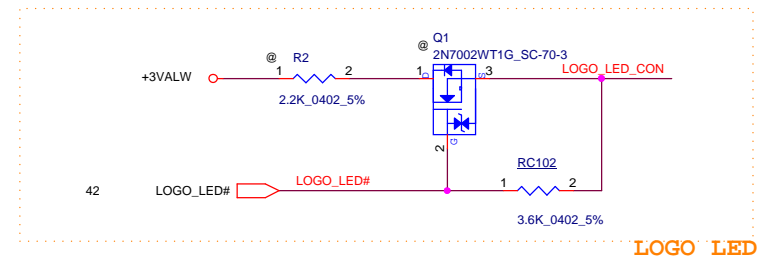
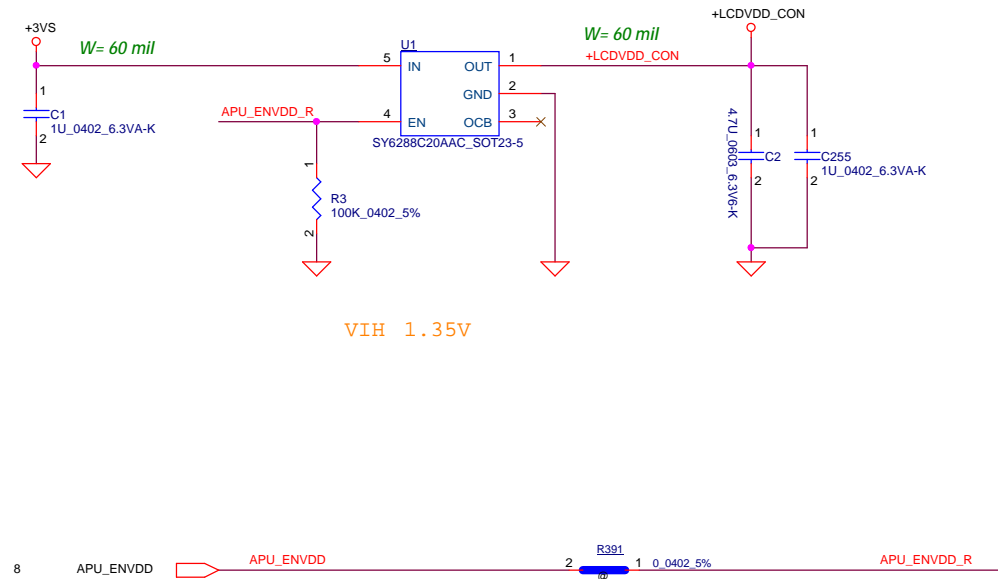
74	3.3V	75	3.3V
72	3.3V	73	3.3V
70	3.3V	71	3.3V
68	SUSCLK (12MHz) (0V/3.3V)	69	PEDET (NC-PCIE)
	Module Key		Module Key
	Module Key		Module Key
	Module Key		Module Key
	Module Key		Module Key
58	Reserved for MFG Clock	57	3.3V
56	Reserved for MFG Data	55	3.3V
54	PERWAKE# (IO)(3.3V)	53	3.3V
52	CLKREQ# (IO)(3.3V)	51	3.3V
50	PERST# (IO)(3.3V)	49	3.3V
48	N/C	47	3.3V
46	N/C	45	3.3V
44	N/C	43	3.3V
42	N/C	41	3.3V
40	N/C	39	3.3V
38	DEVSLP#	37	3.3V
36	N/C	35	3.3V
34	N/C	33	3.3V
32	N/C	31	3.3V
30	N/C	29	3.3V
28	N/C	27	3.3V
26	N/C	25	3.3V
24	N/C	23	3.3V
22	N/C	21	3.3V
20	N/C	19	3.3V
	Module Key		Module Key
	Module Key		Module Key
	Module Key		Module Key
	Module Key		Module Key
35	DAS/DSS# (IO)	34	N/C
33	N/C	32	N/C
31	N/C	30	N/C
29	N/C	28	N/C
27	N/C	26	N/C
25	N/C	24	N/C
23	N/C	22	N/C
21	N/C	20	N/C
19	N/C	18	N/C
17	N/C	16	N/C
15	N/C	14	N/C
13	N/C	12	N/C
11	N/C	10	N/C
9	N/C	8	N/C
7	N/C	6	N/C
5	N/C	4	N/C
3	N/C	2	N/C
1	N/C	0	N/C



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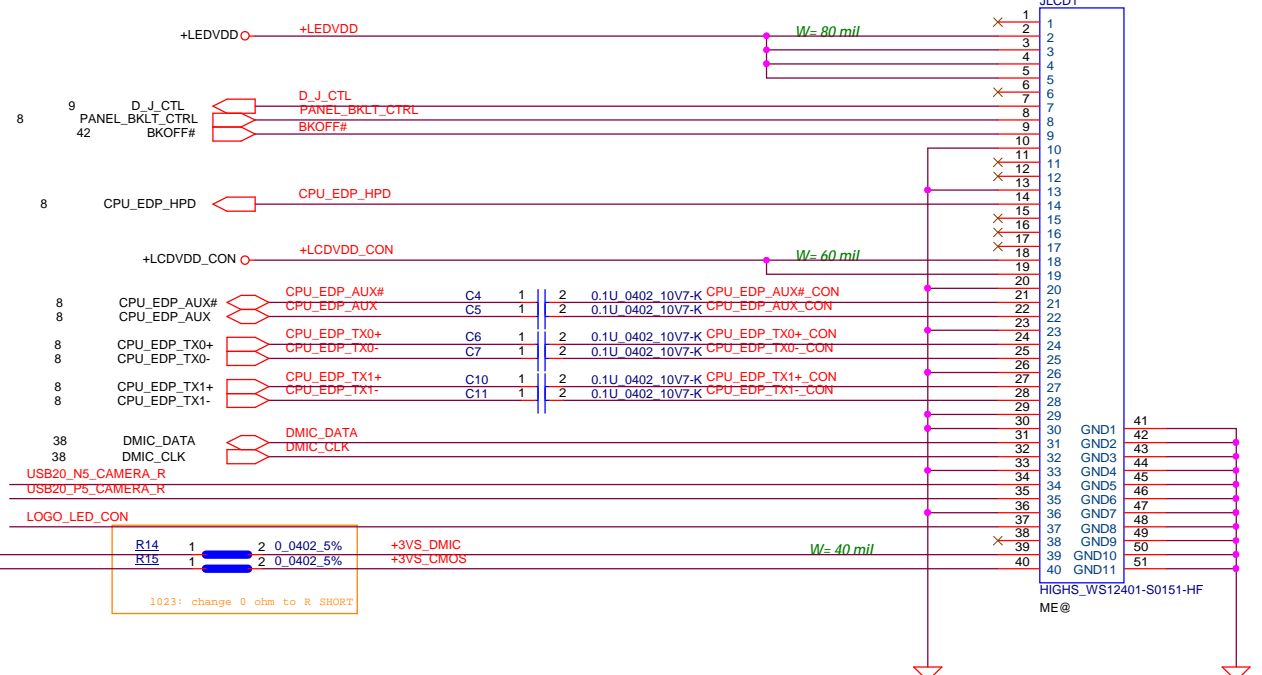
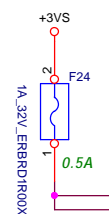
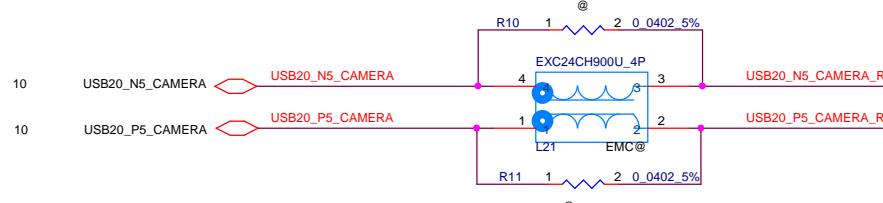
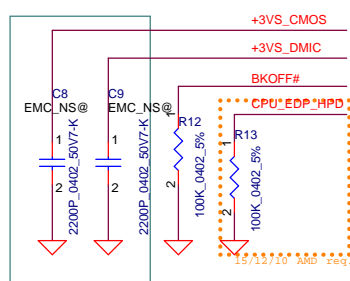
LCDVDD Circuit



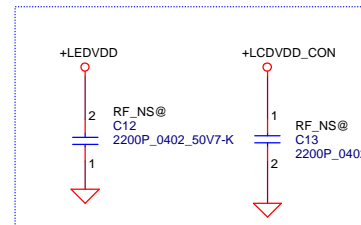
	Dooku	JINN
D_J_CTL	leave as NC	connect to GND by EDP cable

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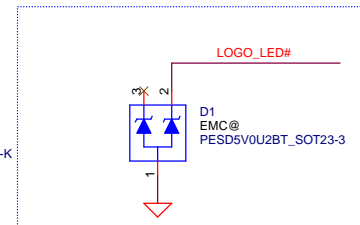
eDP/CMOS/LOGO-LED CONN.



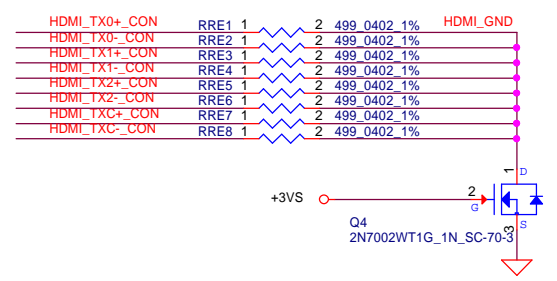
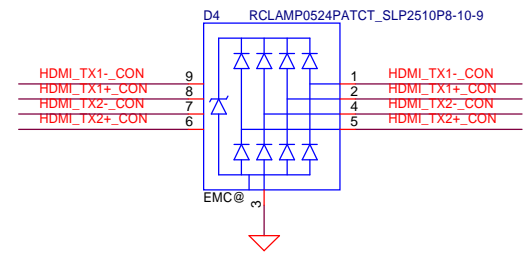
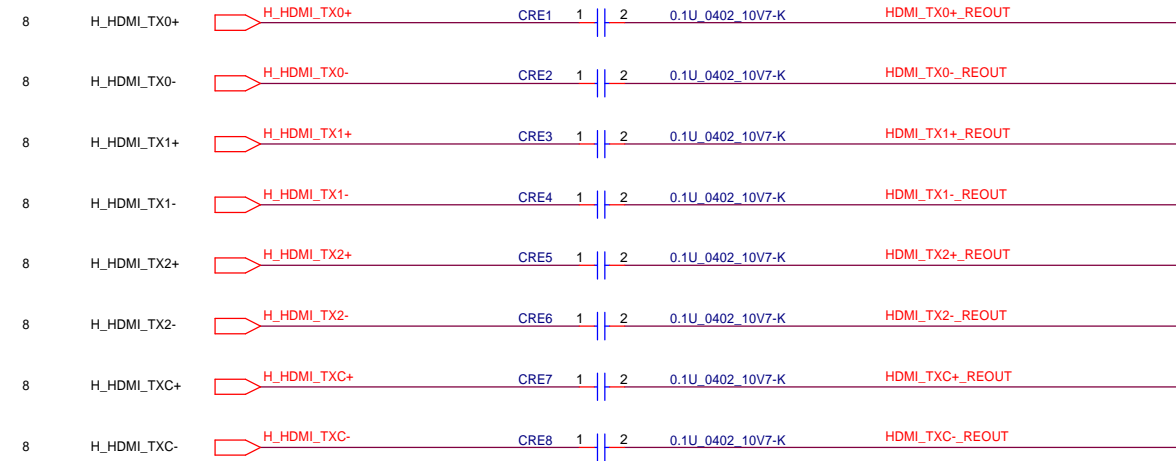
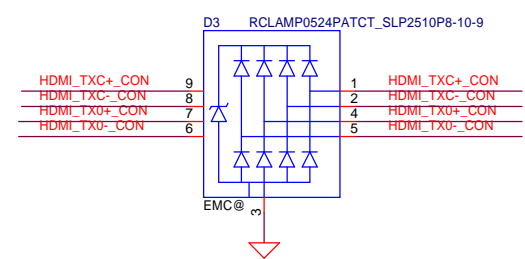
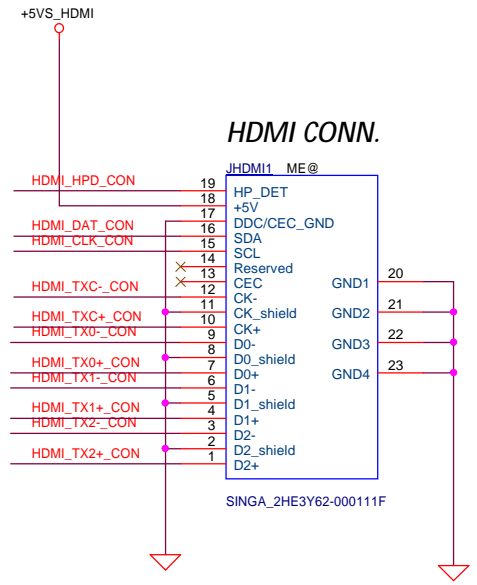
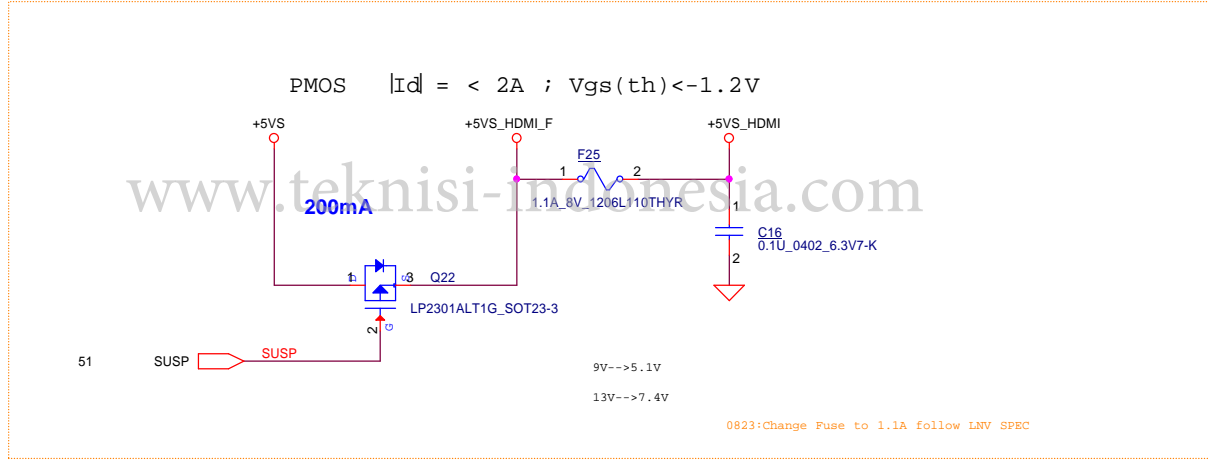
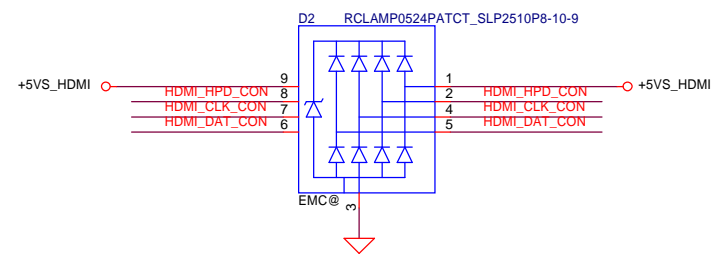
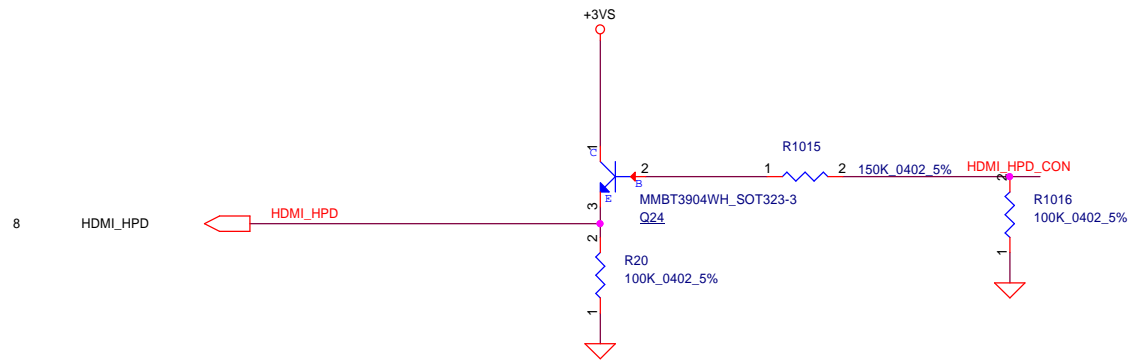
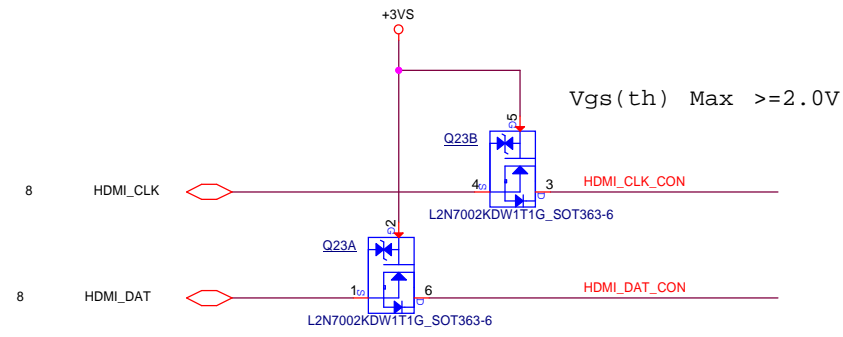
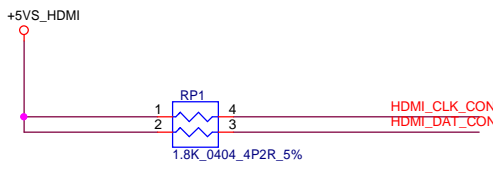
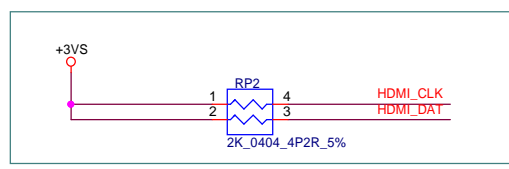
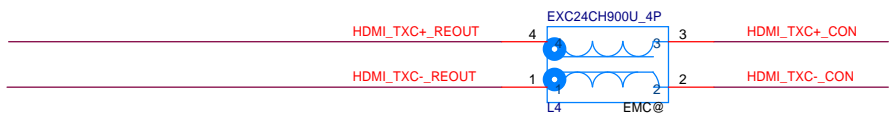
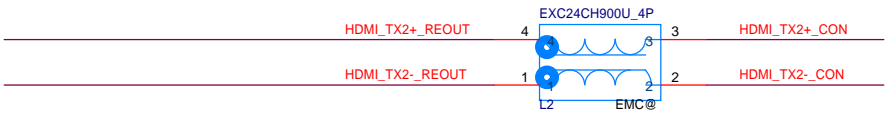
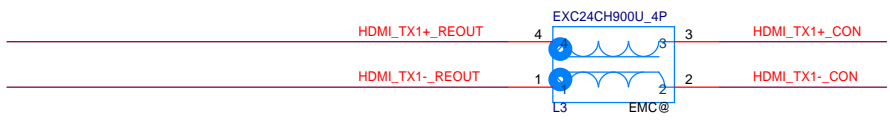
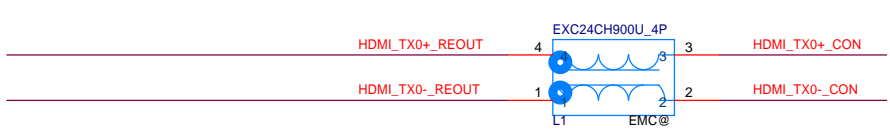
EMC request. Close to JLCD



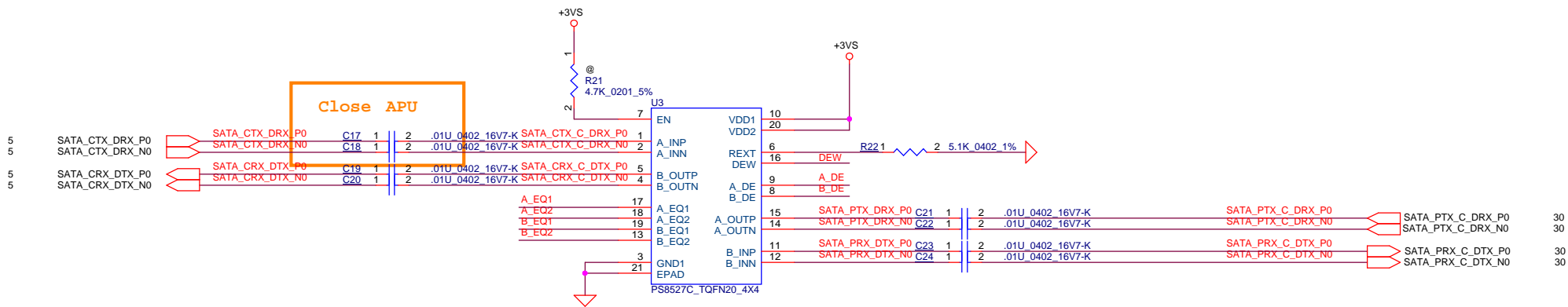
ESD request



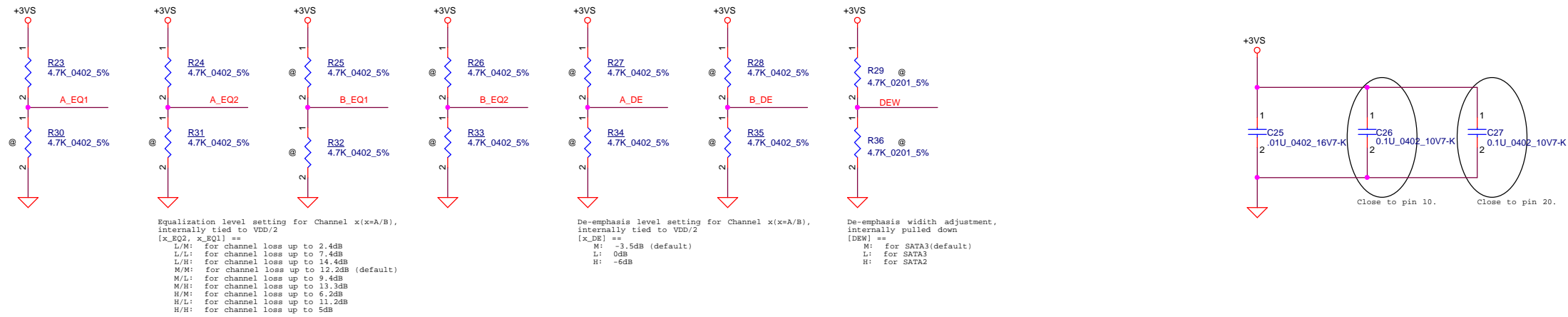
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SATA HDD Redriver

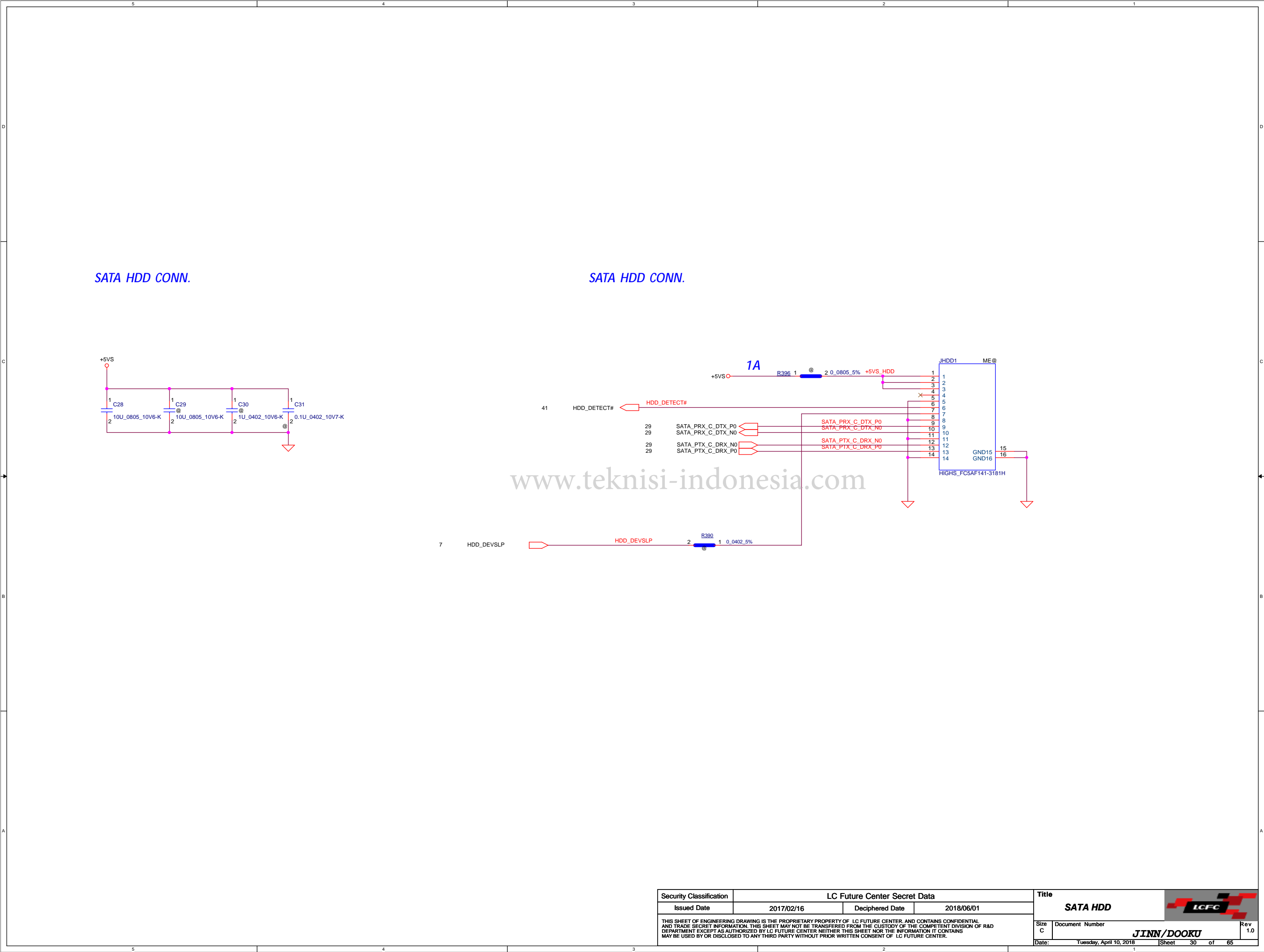


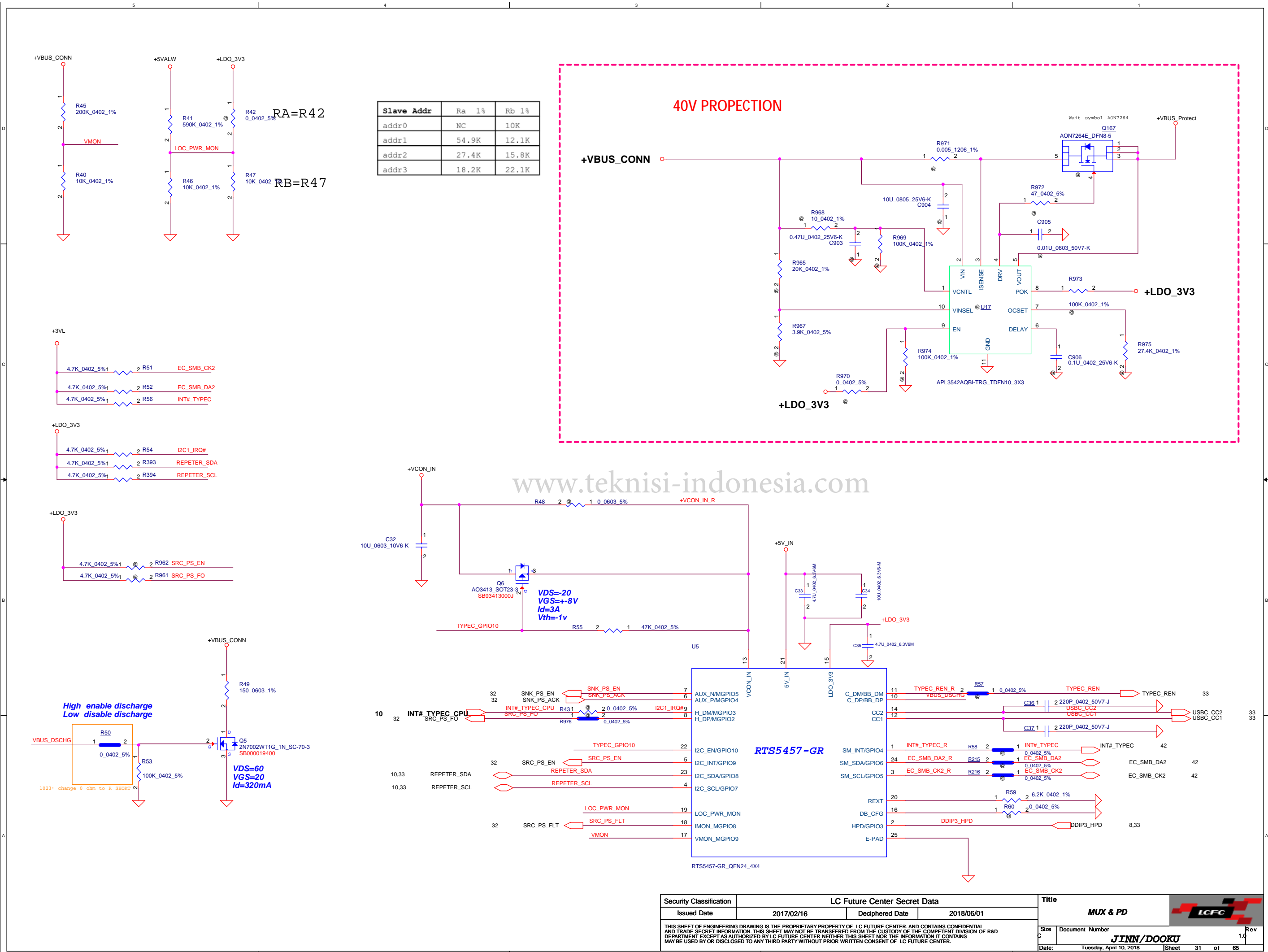
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Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

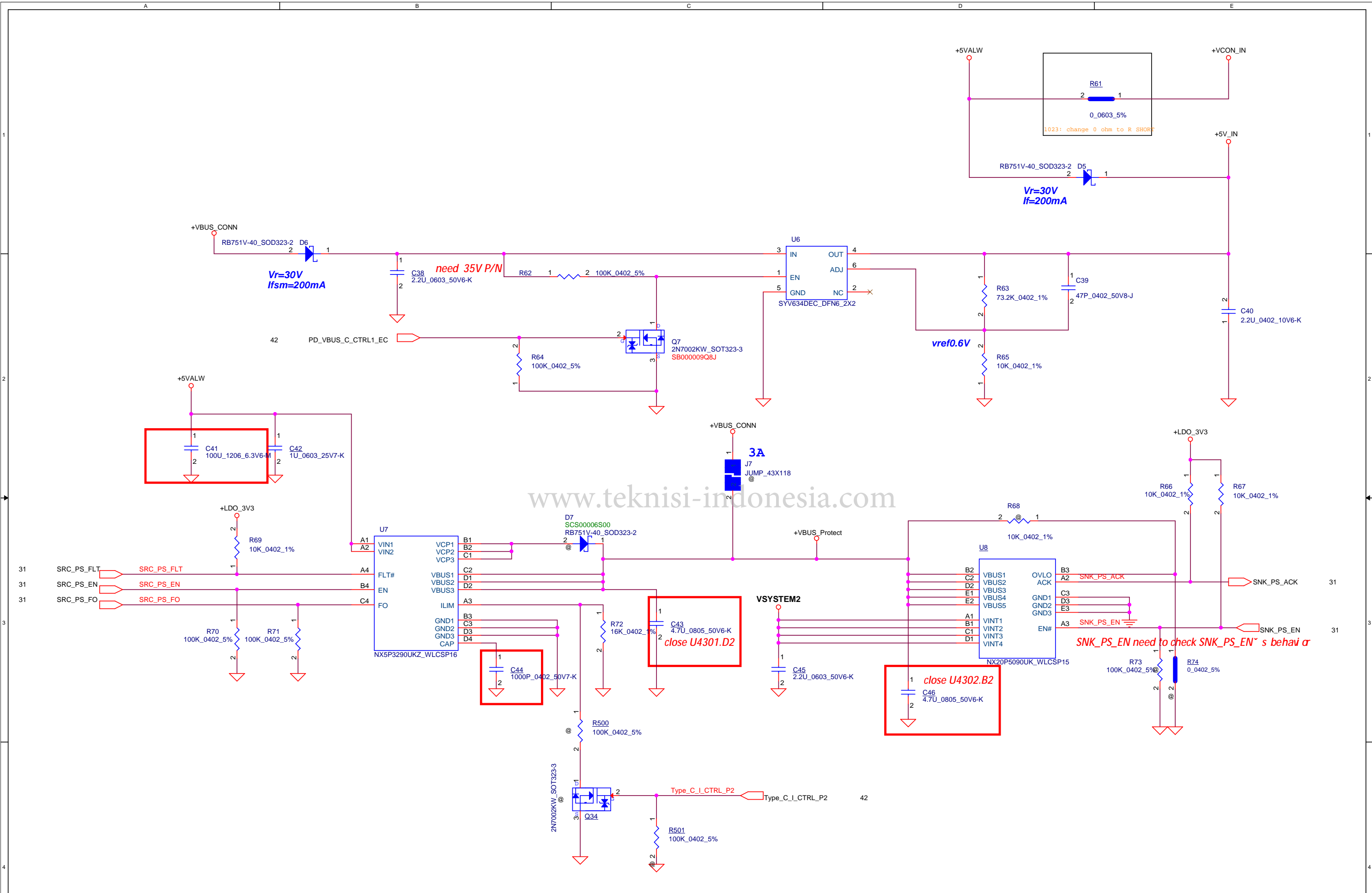
40V PROTECTION

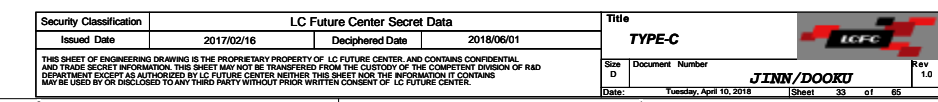
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RTS5457-GR

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MUX & PD		Rev
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C				C																																			
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<table><tr><td>Security Classification</td><td colspan="3">LC Future Center Secret Data</td><td>Title</td></tr><tr><td>Issued Date</td><td>2017/02/16</td><td>Deciphered Date</td><td>2018/06/01</td><td>Switch</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td>Size Custom</td></tr><tr><td colspan="4"></td><td>Document Number JINN/DOOKU</td></tr><tr><td colspan="4"></td><td>Rev 1.0</td></tr><tr><td colspan="4"></td><td>Date: Tuesday, April 10, 2018</td></tr><tr><td colspan="4"></td><td>Sheet 34 of 65</td></tr></table>					Security Classification	LC Future Center Secret Data			Title	Issued Date	2017/02/16	Deciphered Date	2018/06/01	Switch	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom					Document Number JINN/DOOKU					Rev 1.0					Date: Tuesday, April 10, 2018					Sheet 34 of 65
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On Board (LEFT-Front)

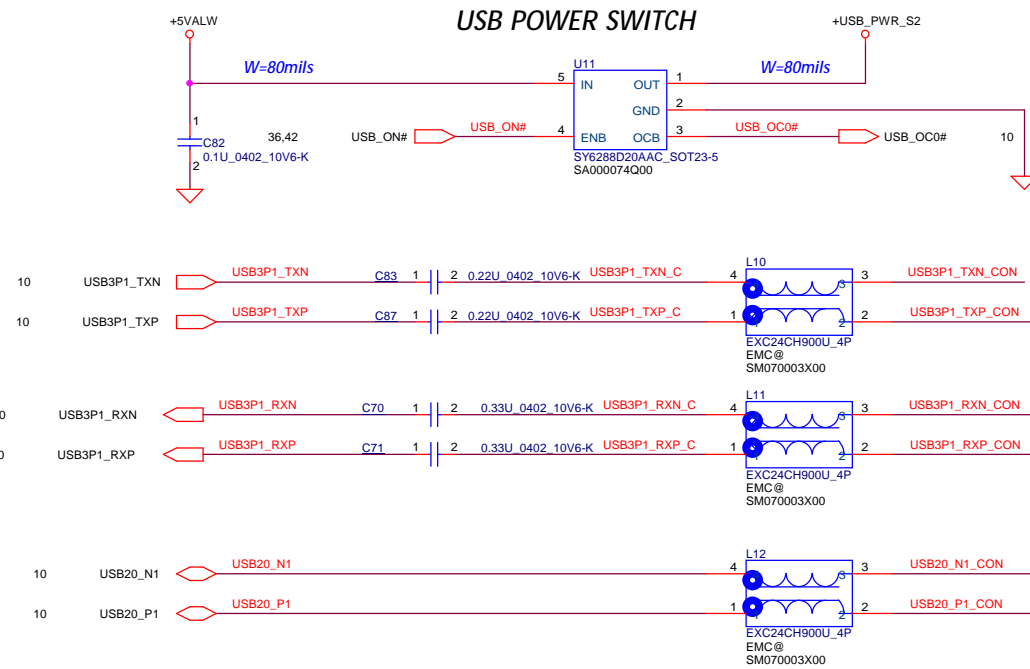
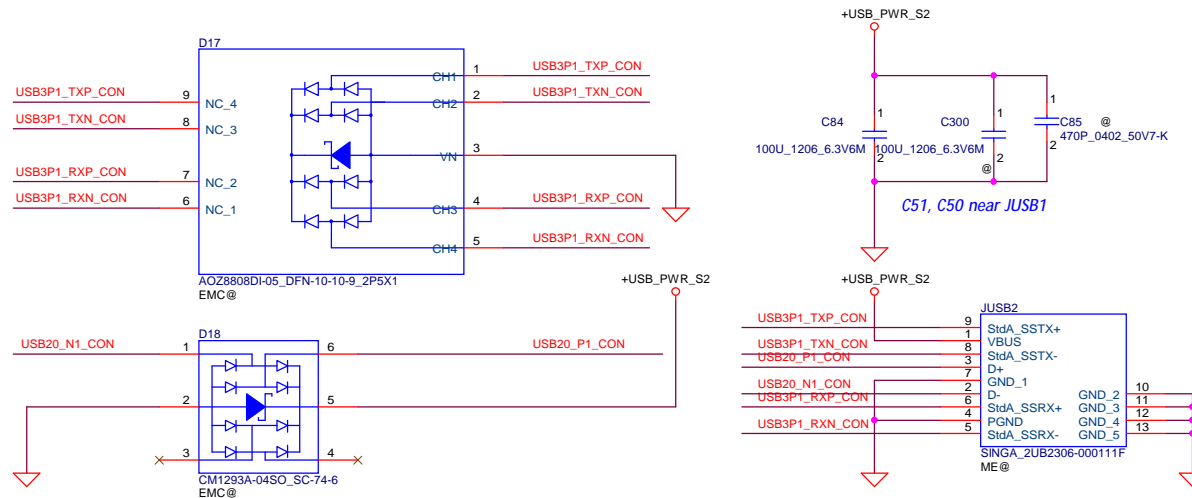
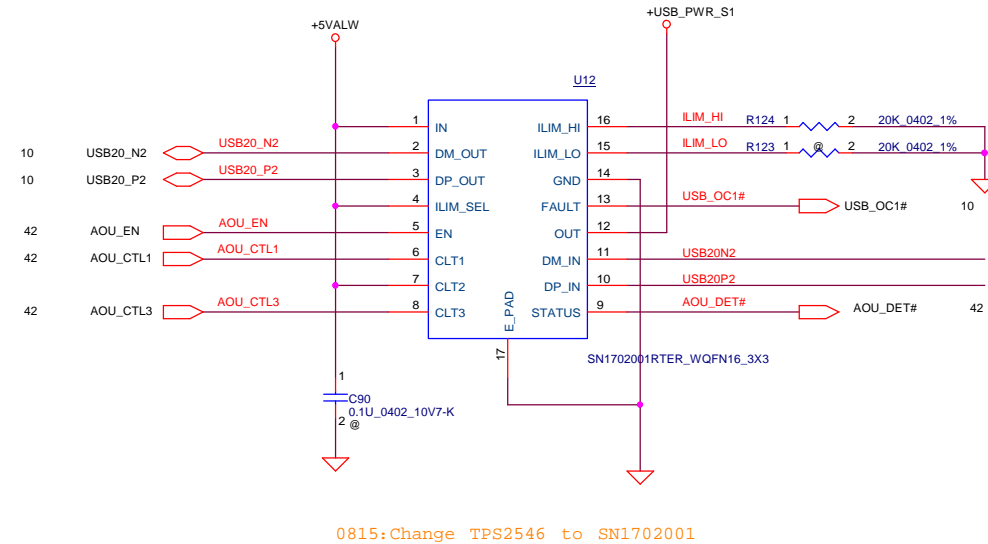


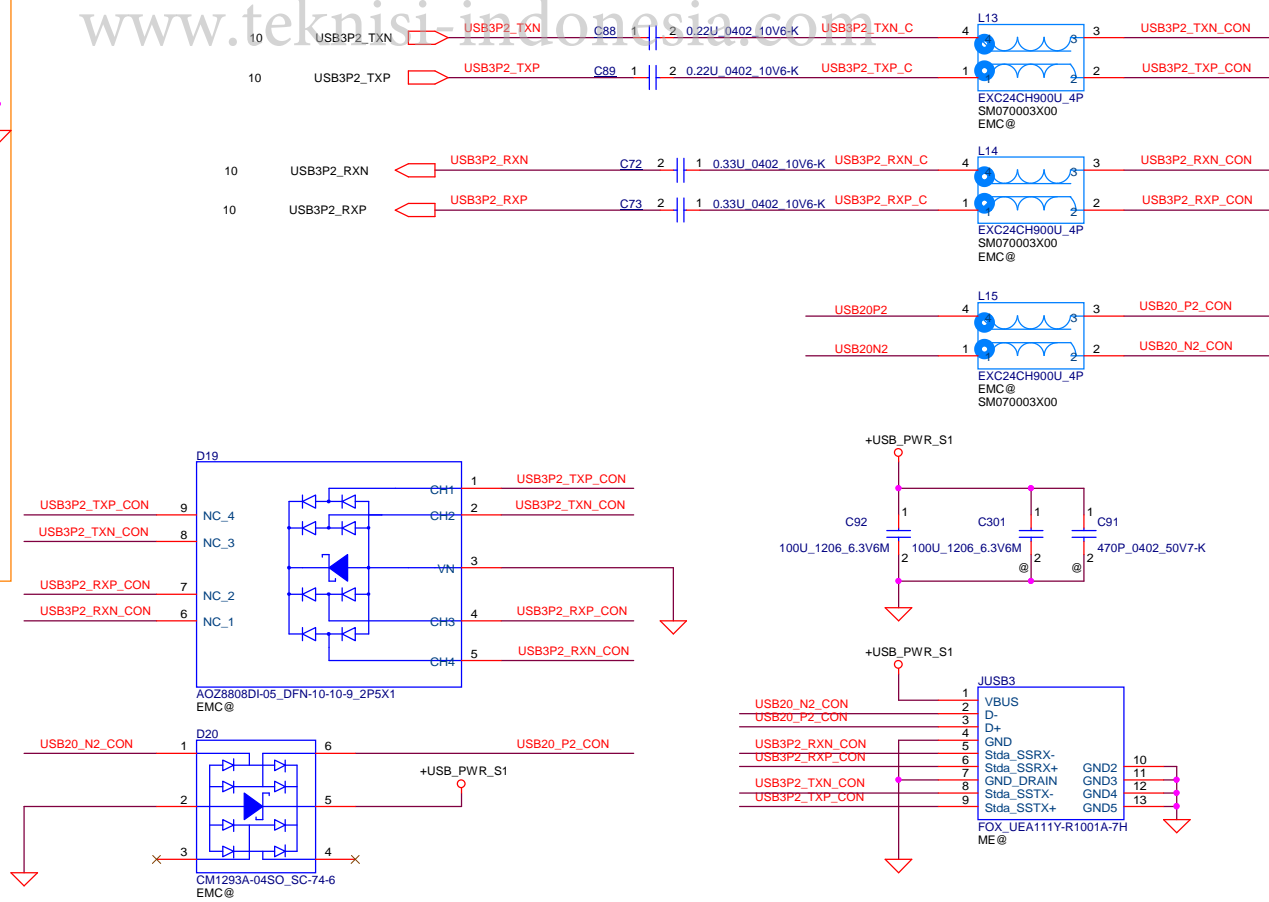
TABLE of POWER SWITCH (U6401)		
Vendor	LCFC P/N	Description
SILERGY	SA000074Q00	S IC SY6288D20AAC SOT23 5P POWER SWITCH
GMT	SA000079400	S IC G517F2T11U SOT-23 5P POWER SWITCH



On Board (LEFT-Back)




0815:Change TPS2546 to SN1702001



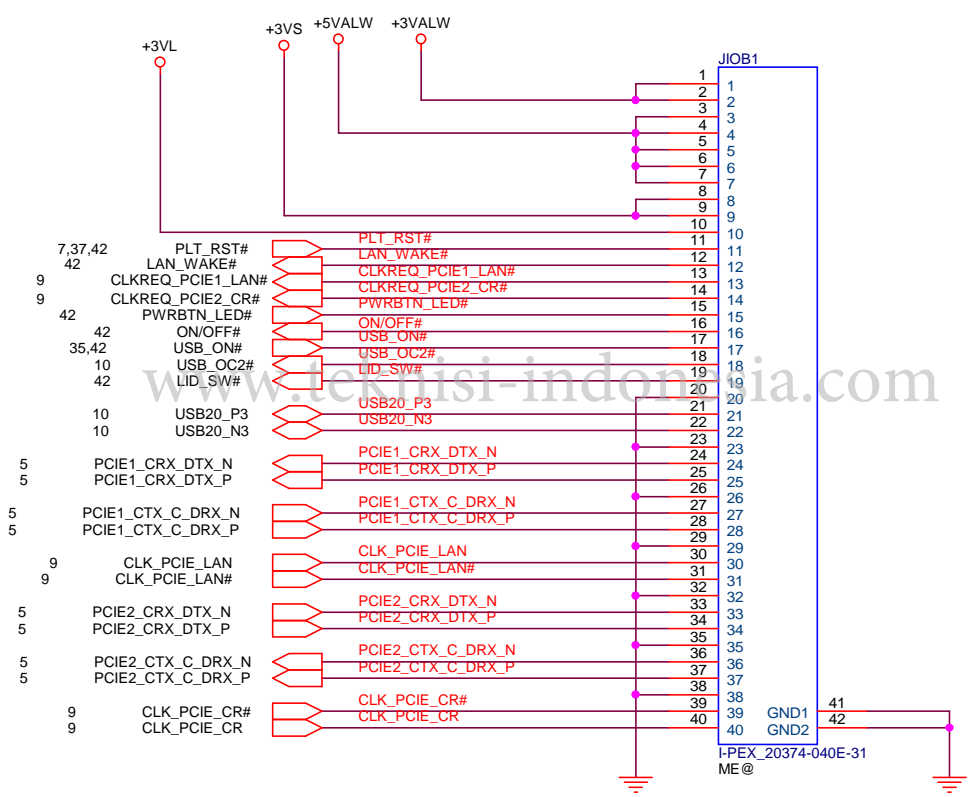
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Title			
USB3 P1/2 CONN.			
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IO_40_Pin conn

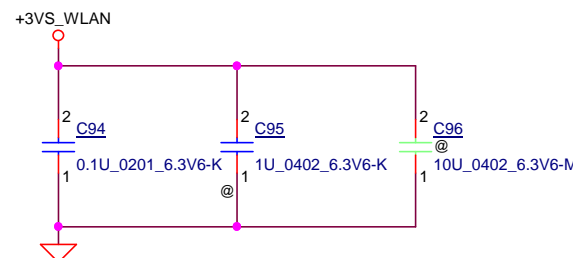
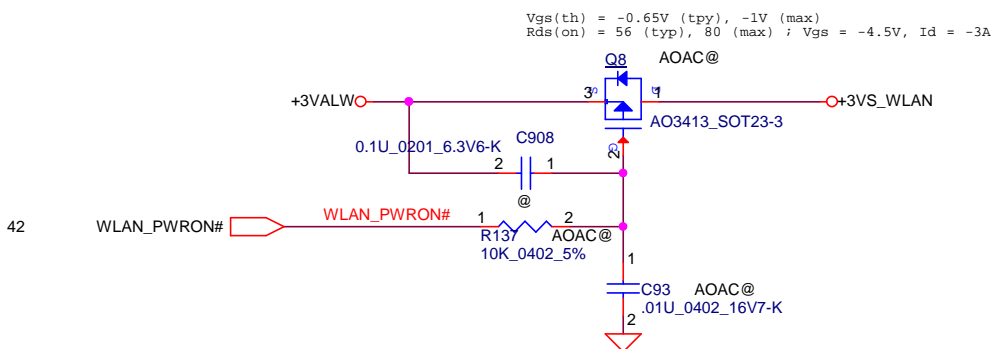
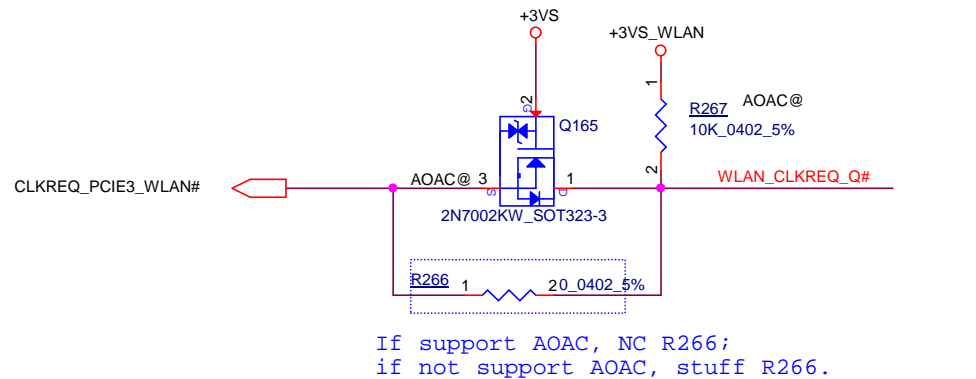
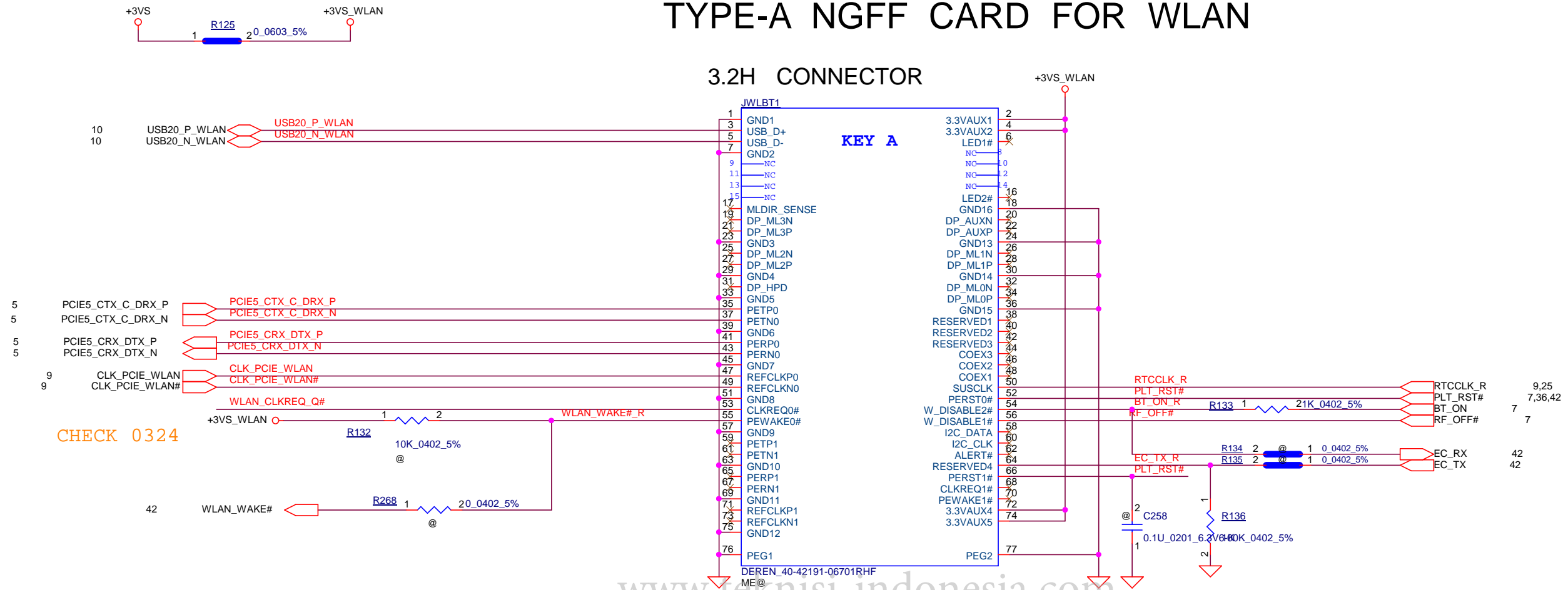
USB2.0
GBE LAN PHY
Card Reader



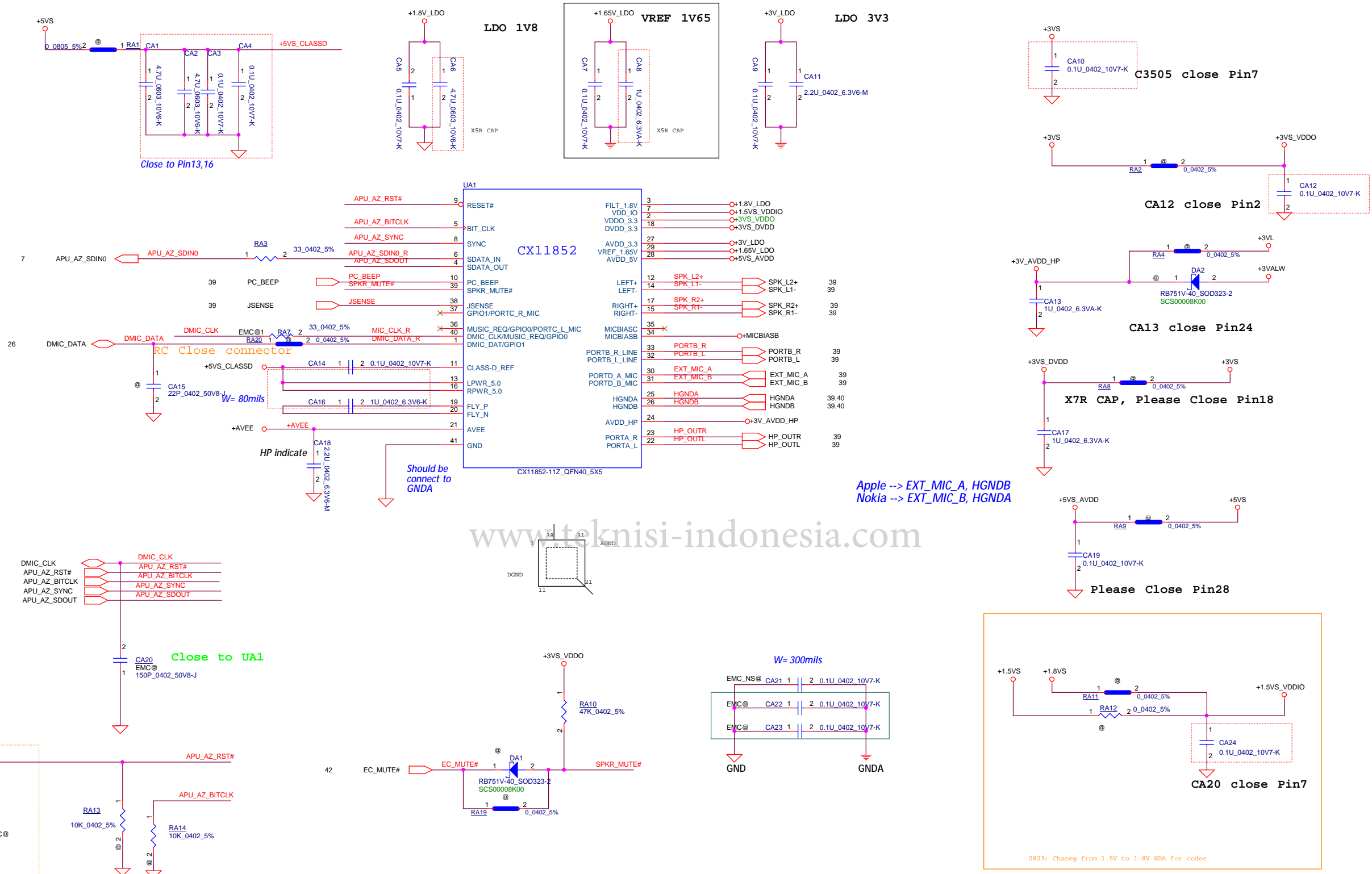
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TYPE-A NGFF CARD FOR WLAN

3.2H CONNECTOR

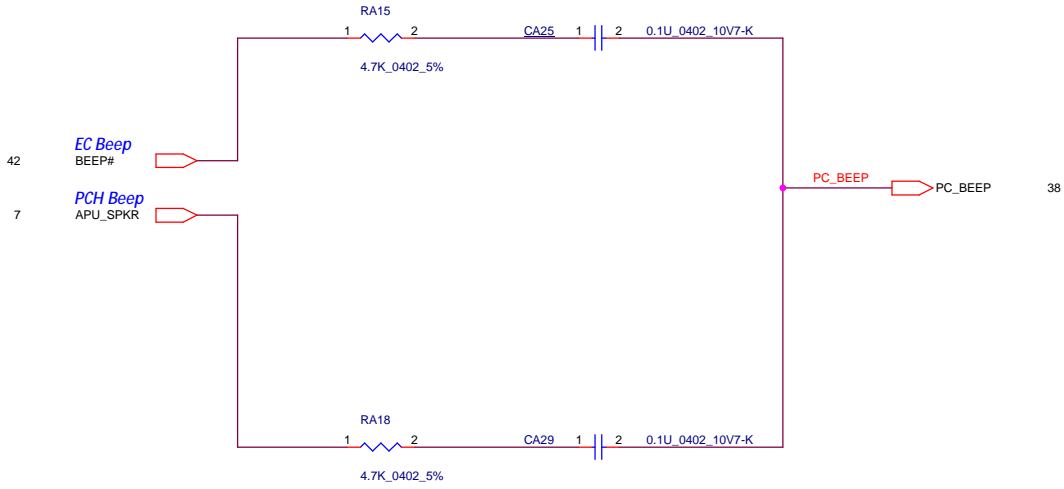


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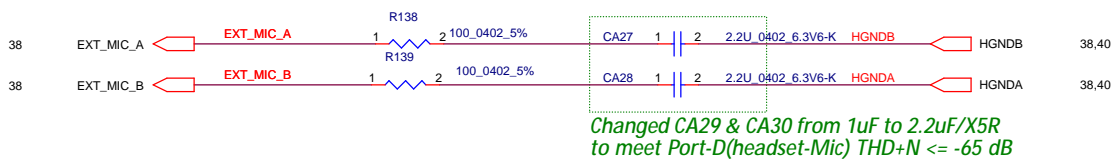


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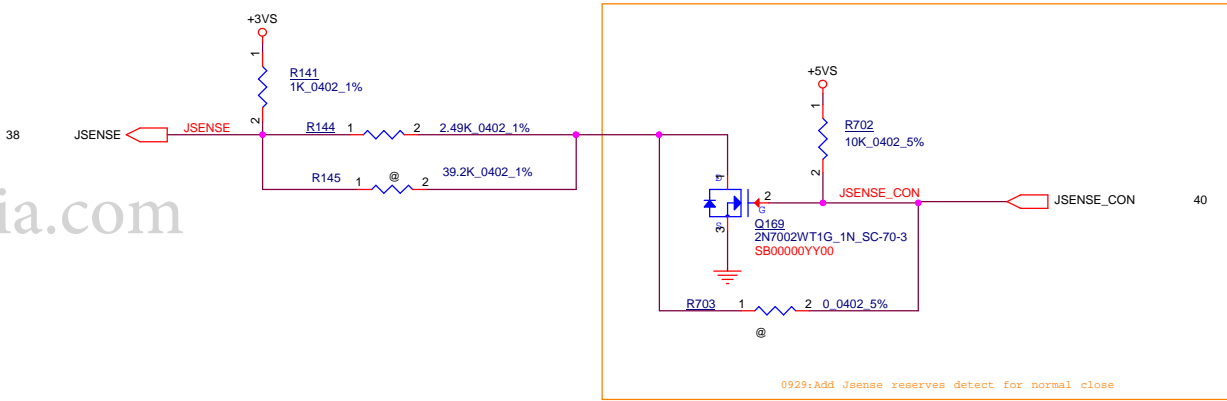
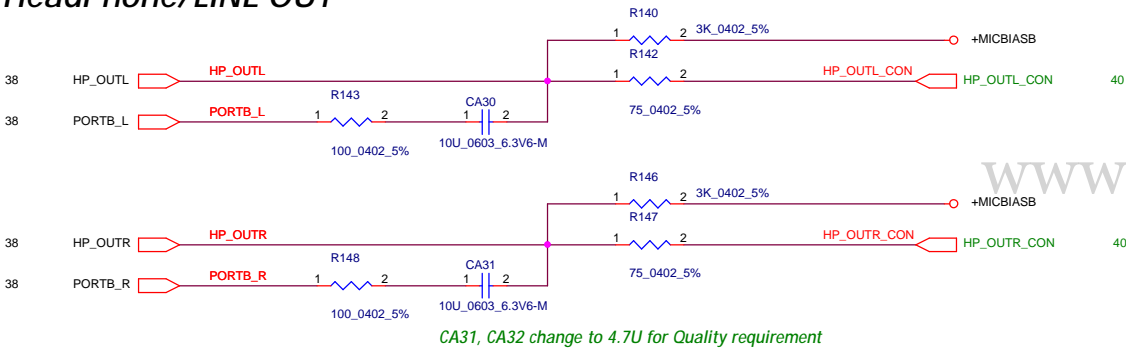
PC Beep



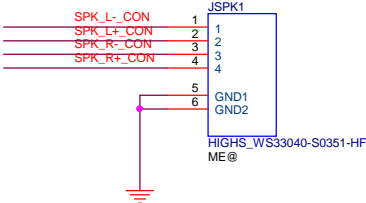
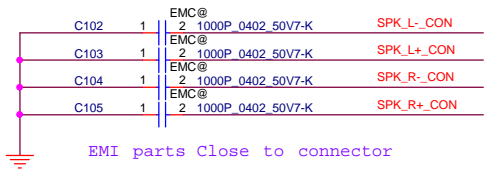
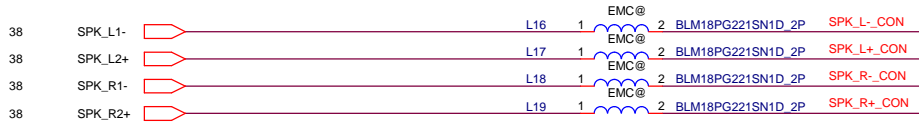
EXT. MIC/LINE IN Apple --> EXT_MIC_A, HGNCB
 Nokia --> EXT_MIC_B, HGNCDA



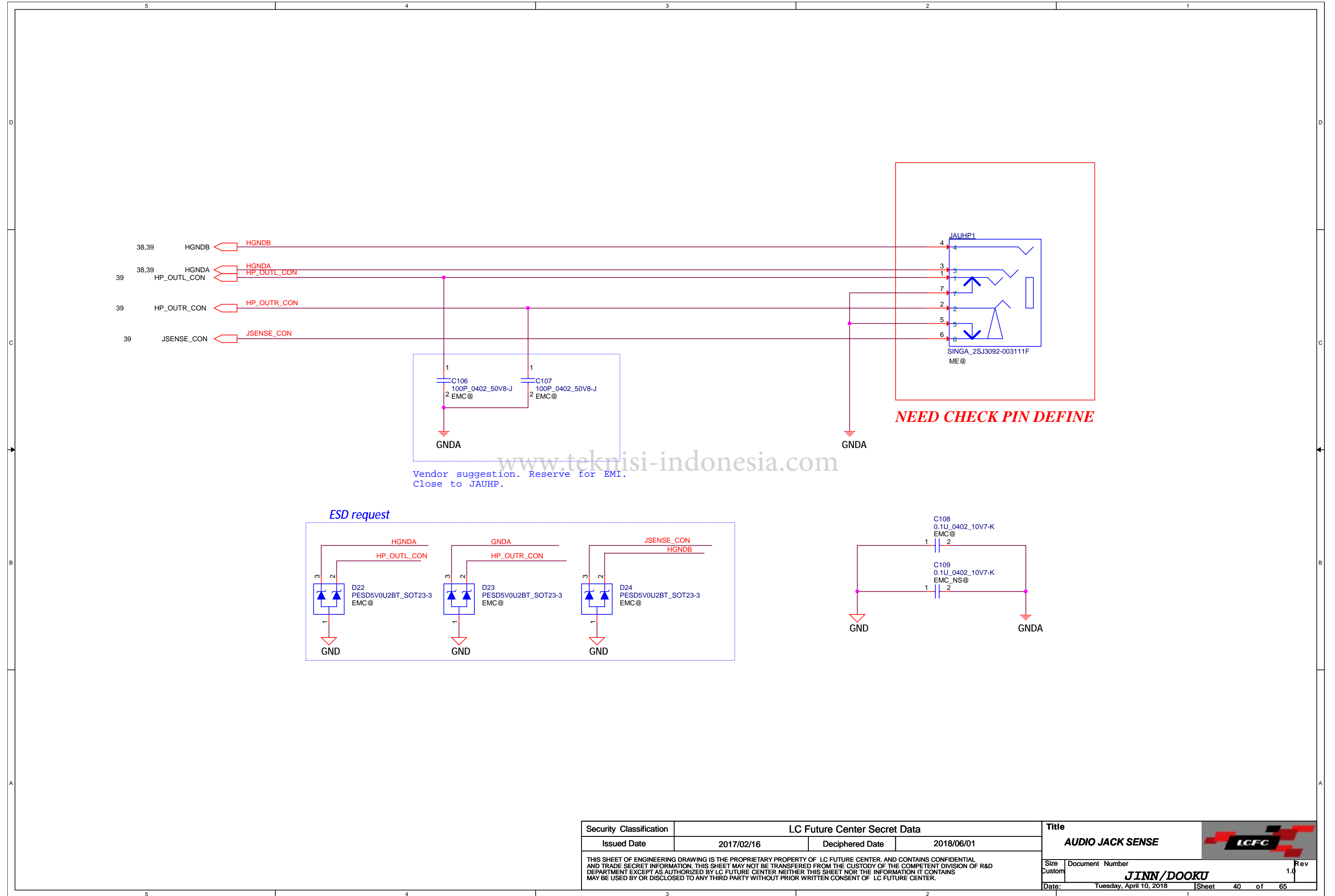
HeadPhone/LINE OUT



SPK CONN.



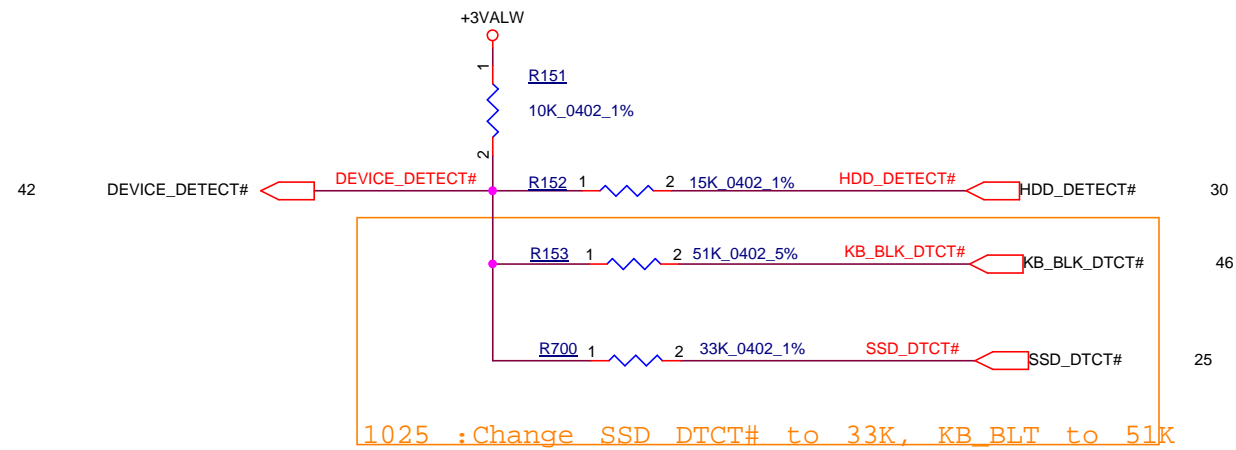
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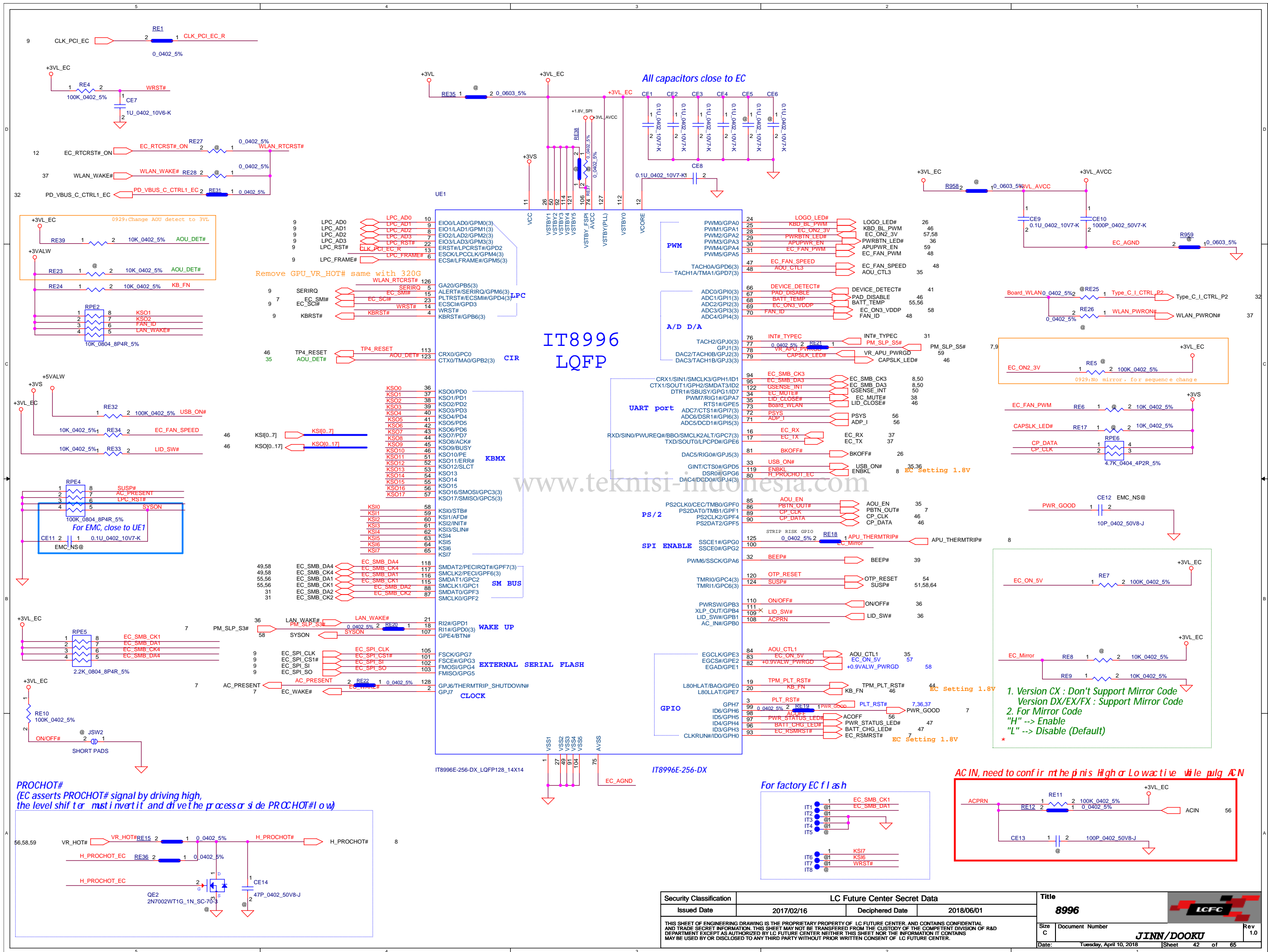


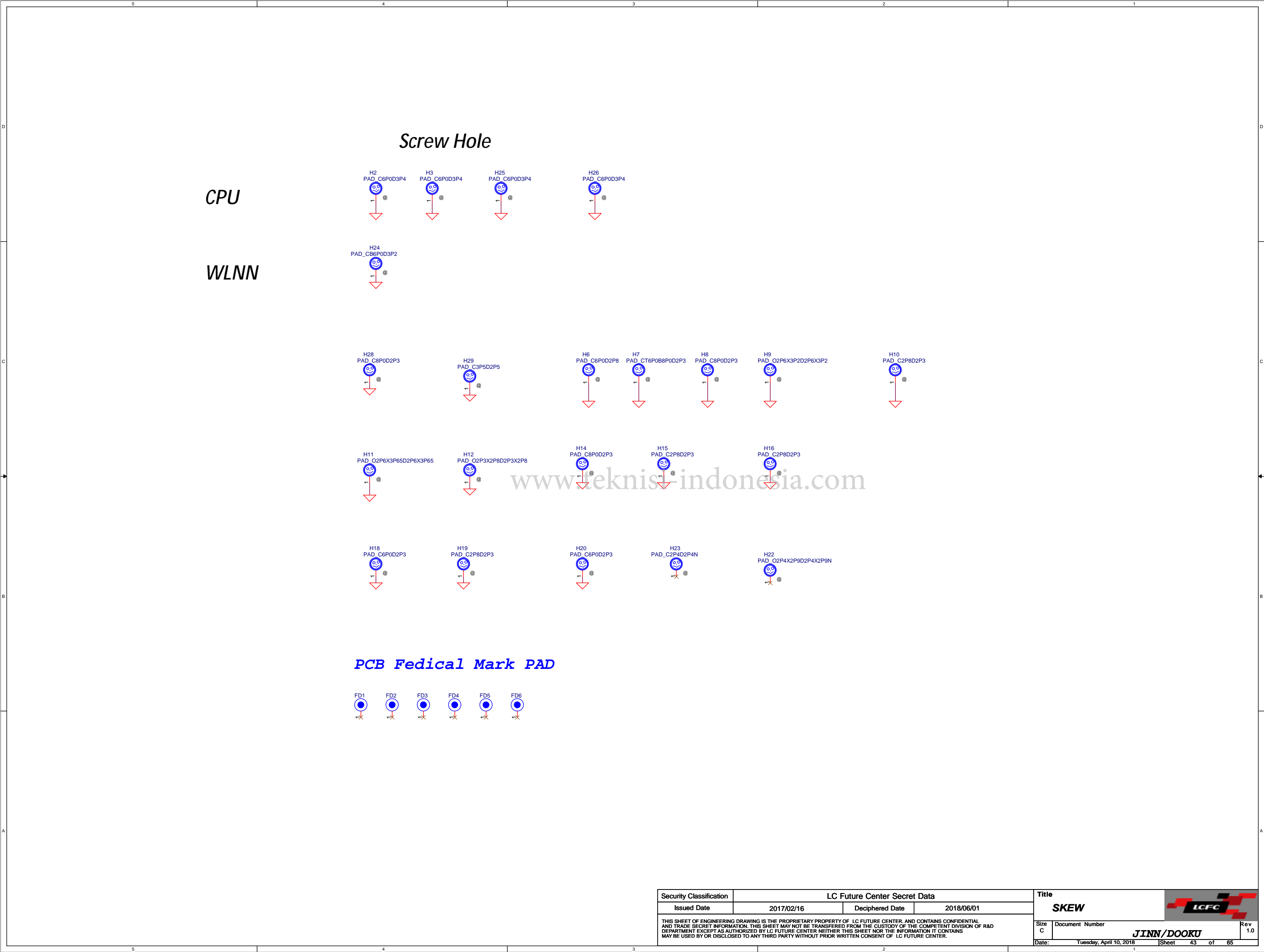
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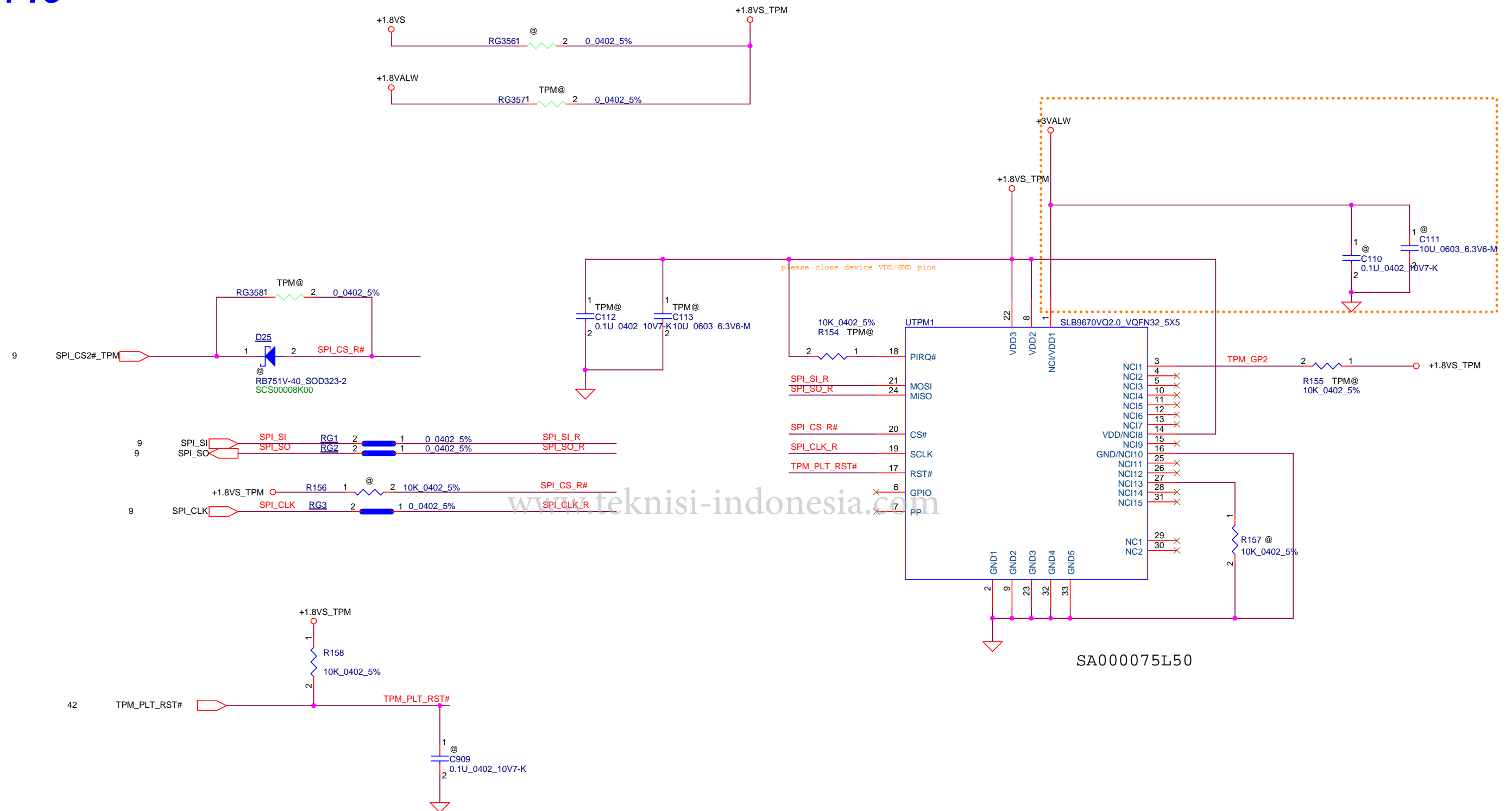
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Vcc	3.3V					
R151	10K +/- 5%					
DEVICE_DETECT1#	1.98V	1.675V	1.772V	2.759V	2.533V	3.3V
HDD_DETECT#	V	V	V	X	X	X
KB_BLK_DTCT#	X	V	X	X	V	X
WWAN_DTCT#	X	X	V	V	X	X

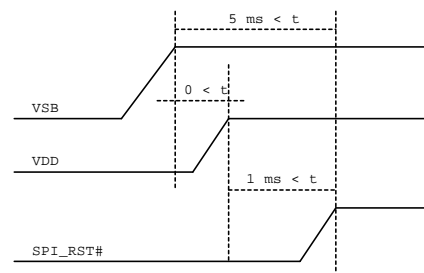




TPM IC



NOTE:
Check timing sequence in SDV phase.



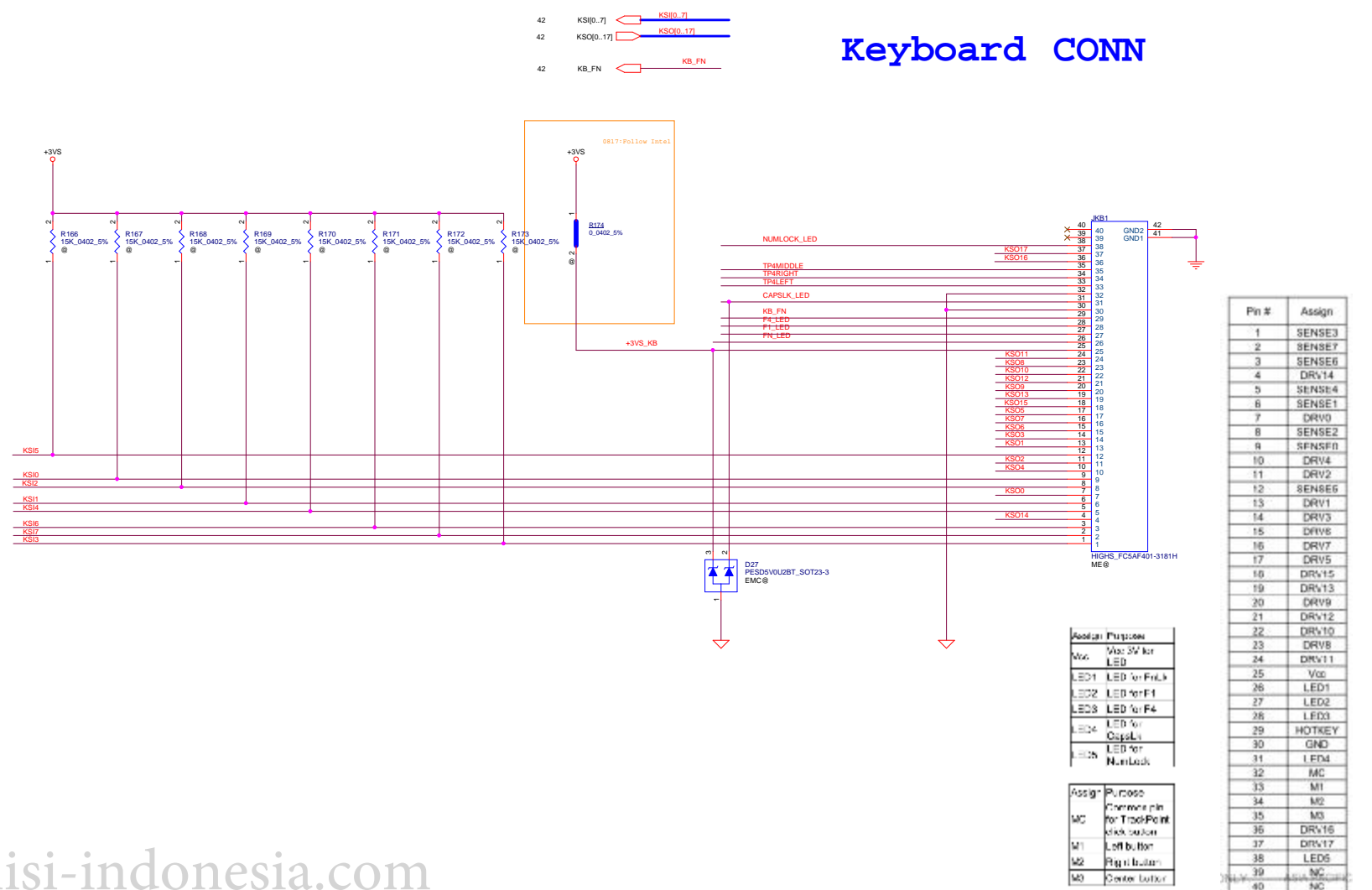
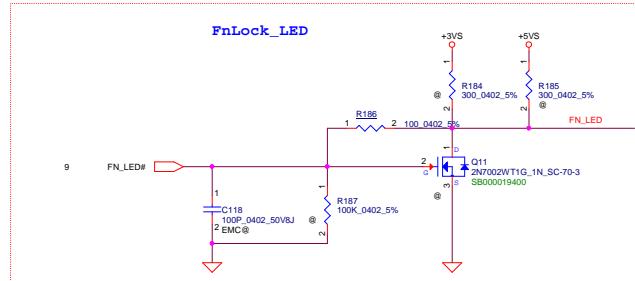
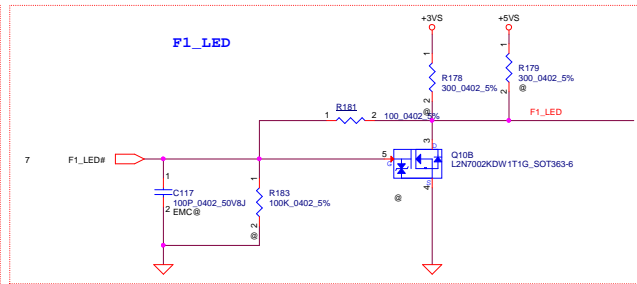
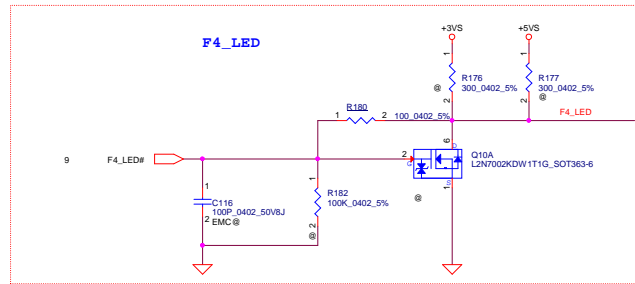
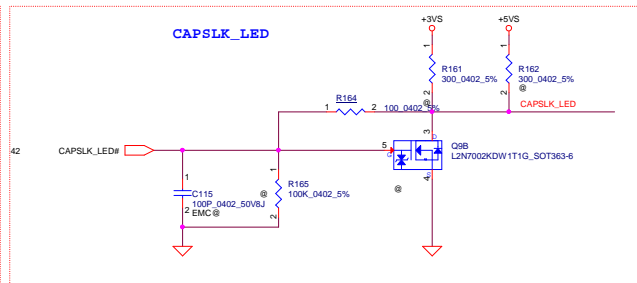
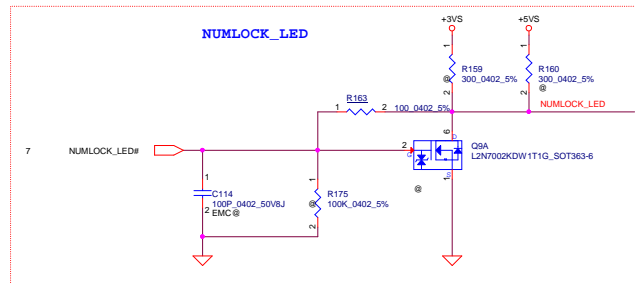
- NOTE:
- 1) It is recommended to connect the TPM to the system's standby voltage to improve performance.
 - 2) SPI_RST# must be asserted for at least 5 msec after VSB power-up.
 - 3) VSB may come up anytime before VDD power-up, but not after VDD power-up.
 - 4) SPI_RST# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

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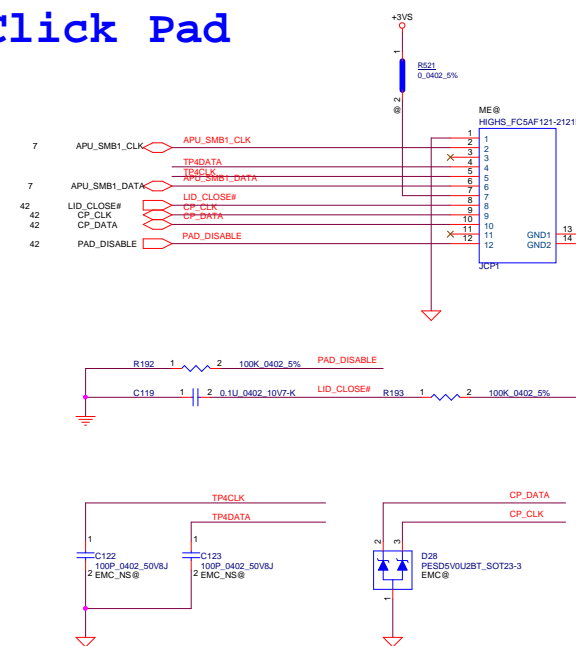
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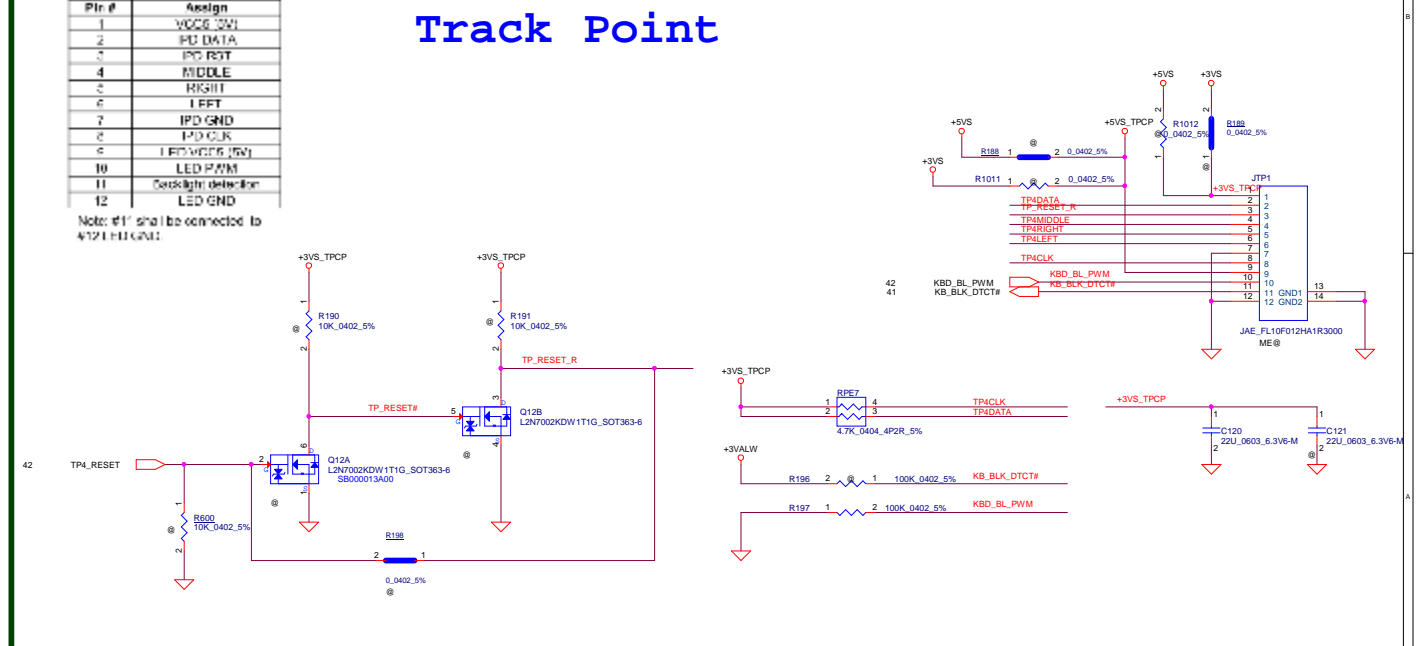


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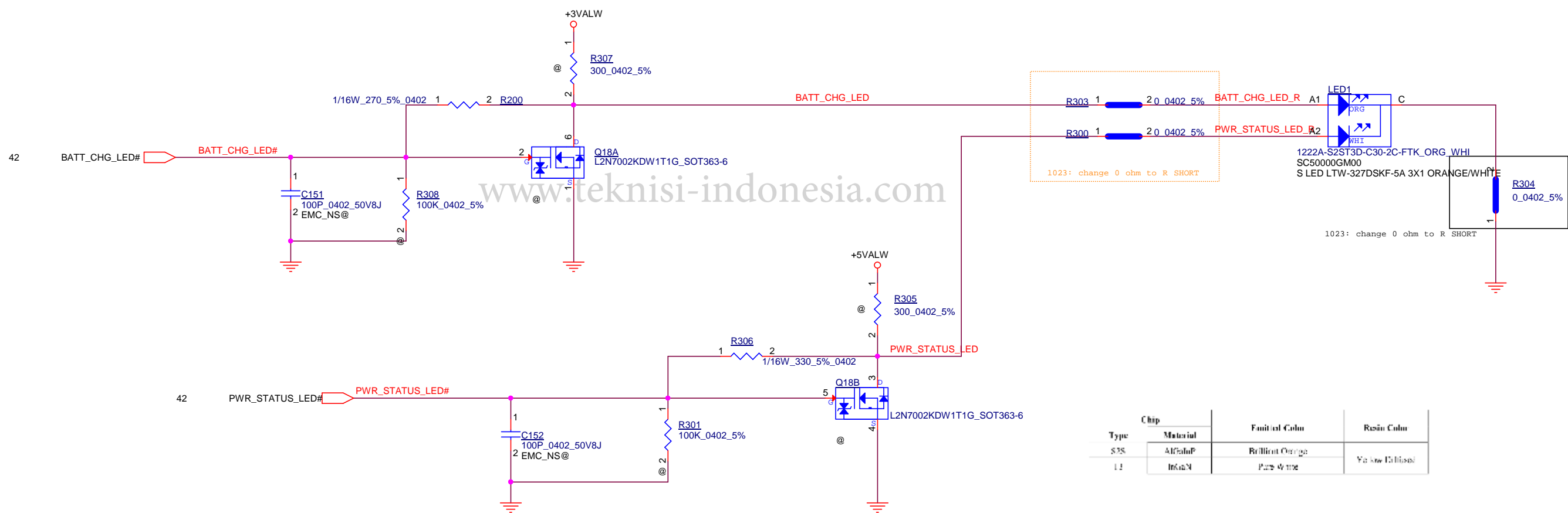
Click Pad




Track Point

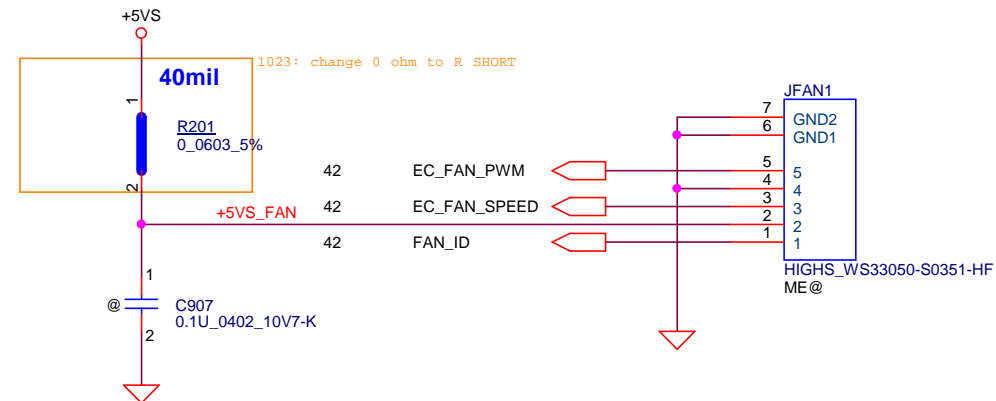


POWER ADAPTER Bi-COLOR(ORANGE/WHITE)



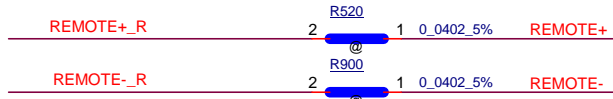
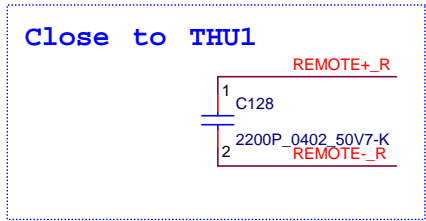
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Issued Date		2017/02/16	Deciphered Date	2018/06/01		POWER LED	
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FAN CONN.



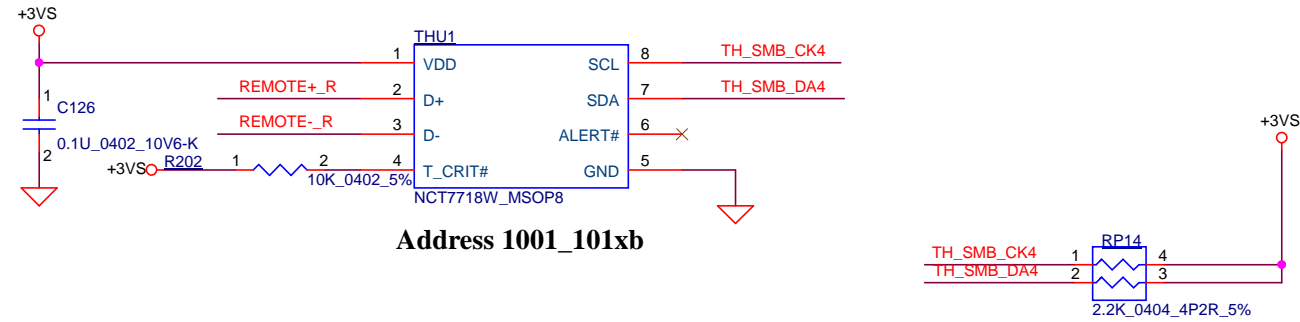
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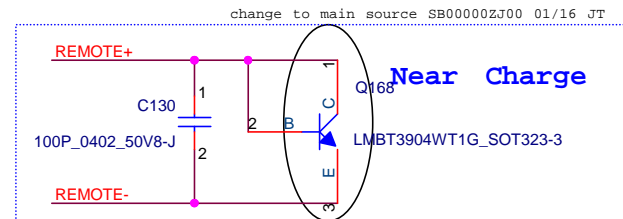


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near APU

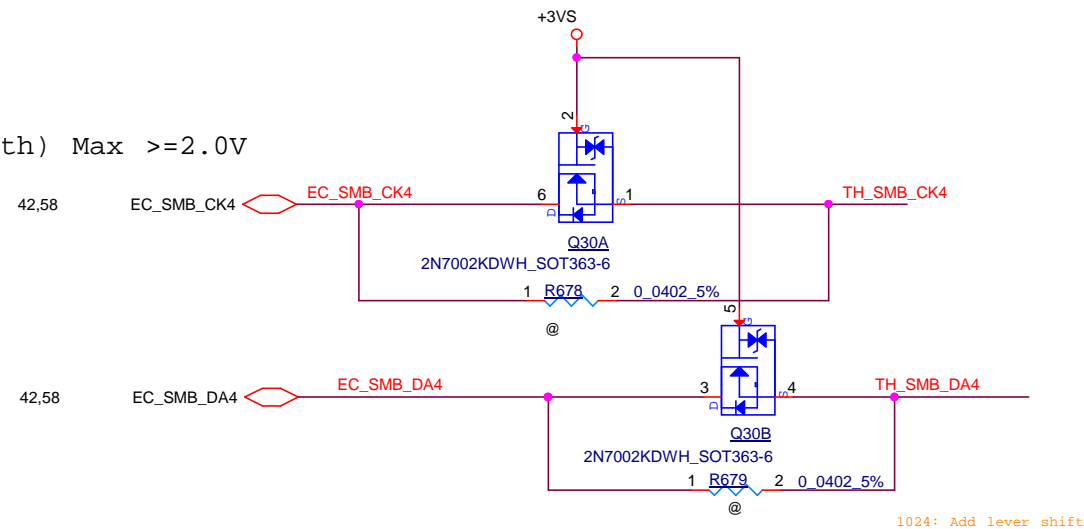


0929:Change Thermal sensor SMB3 to SMB4

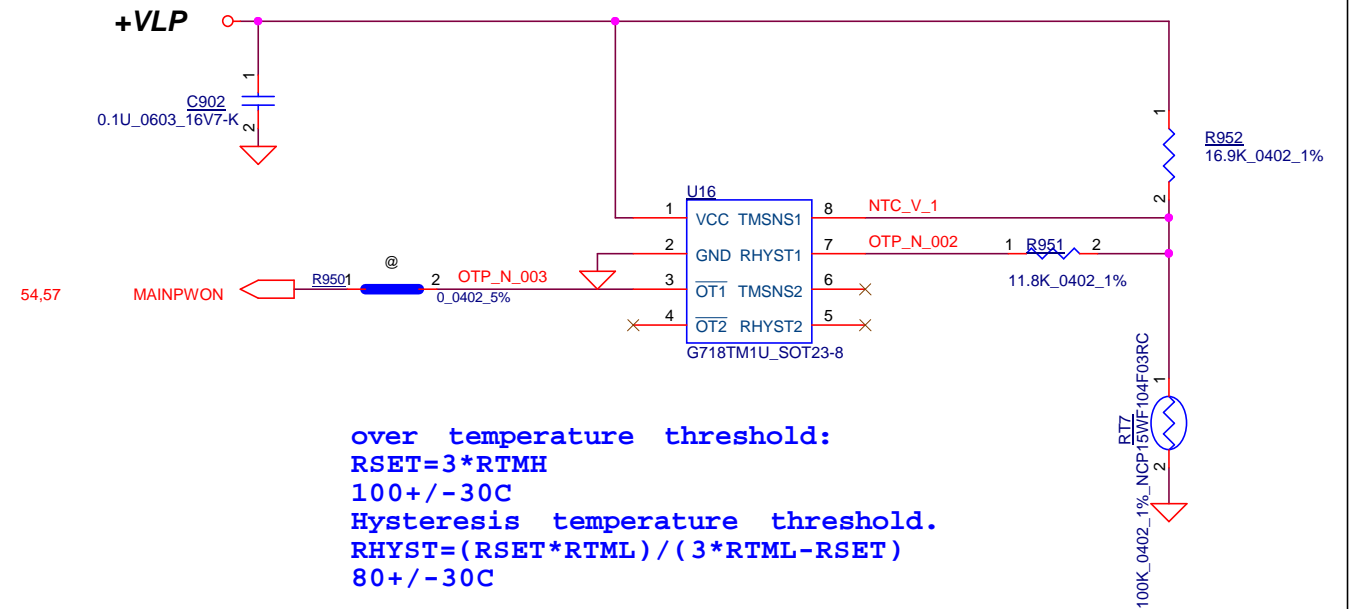


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Vgs(th) Max >=2.0V

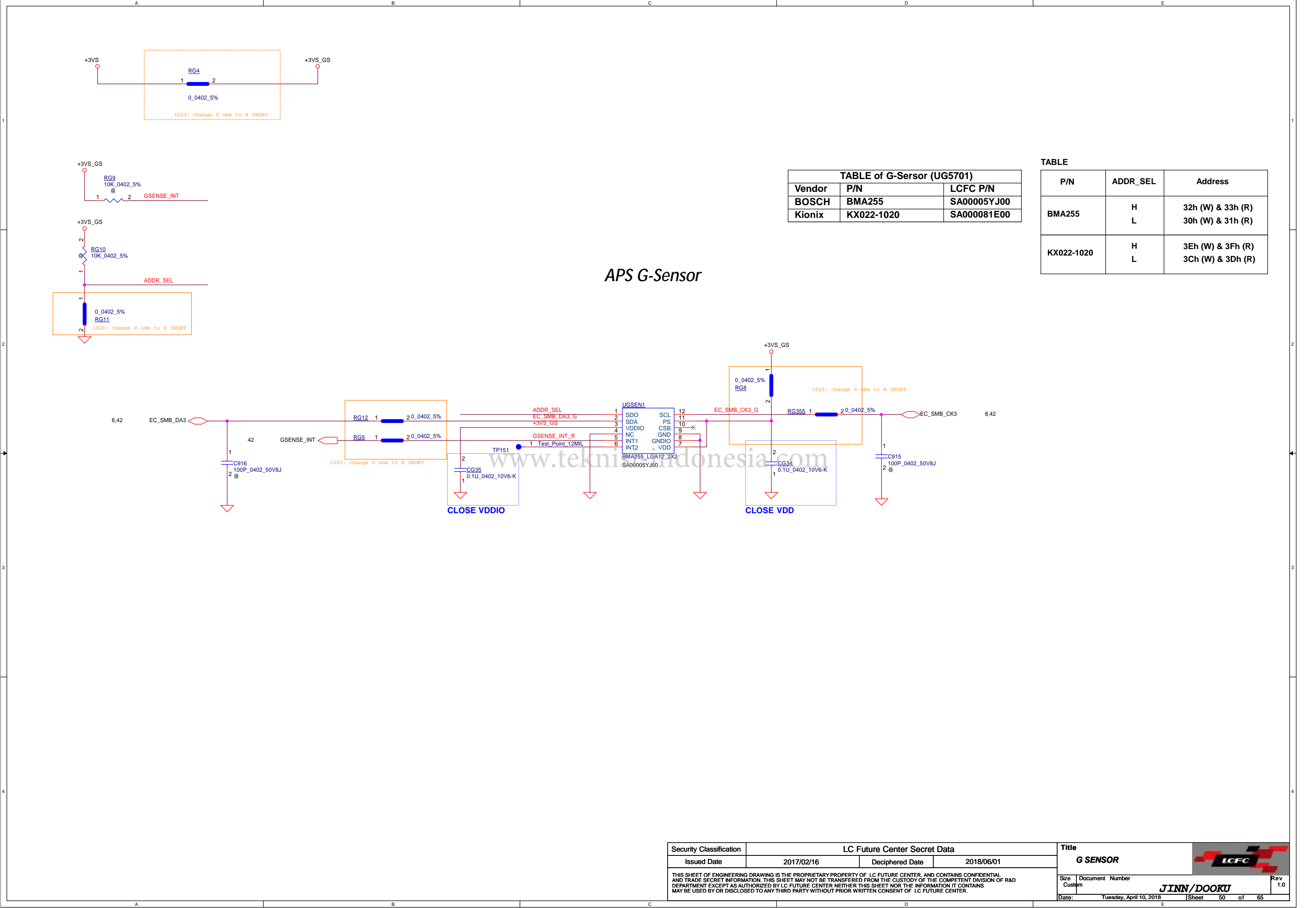


1024: Add lever shift



over temperature threshold:
 $RSET=3*RTMH$
 $100+/-30C$
Hysteresis temperature threshold.
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
 $80+/-30C$

Security Classification	LC Future Center Secret Data			Title Thermal Sensor		
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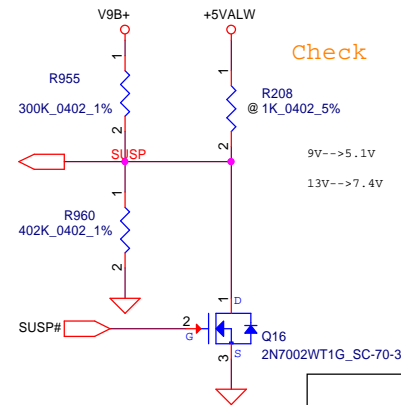


APS G-Sensor

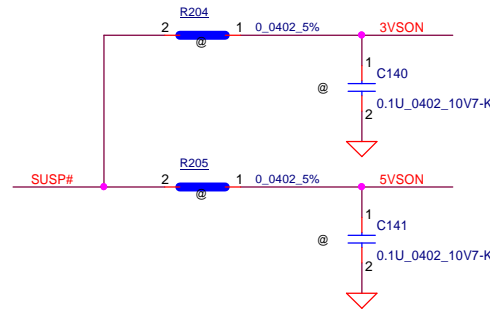
TABLE of G-Sensor (UG5701)		
Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00

TABLE		
P/N	ADDR_SEL	Address
BMA255	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

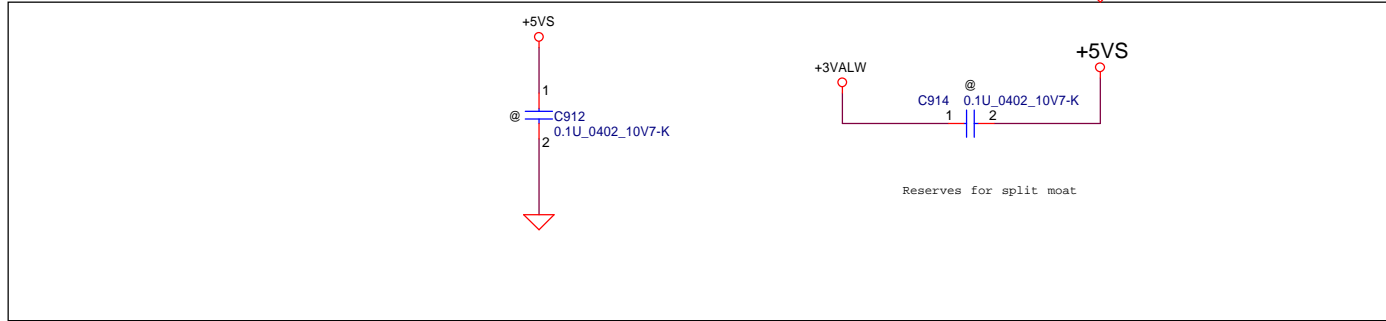
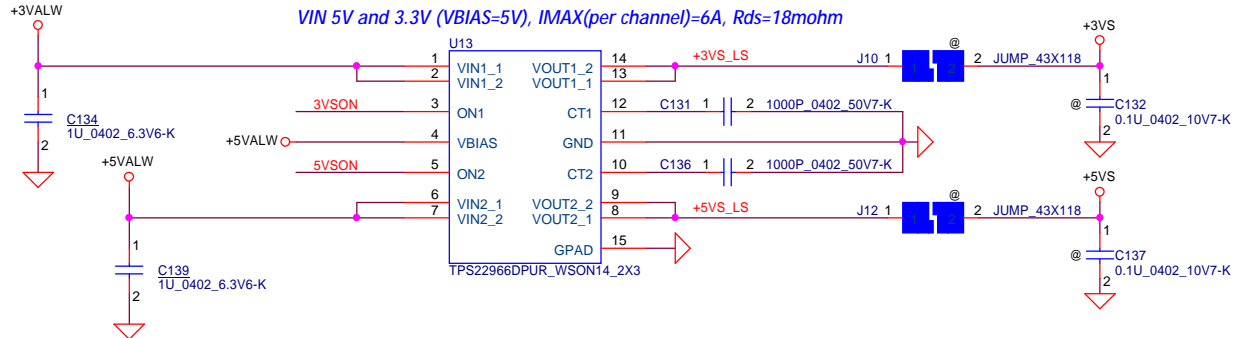
Check 5VLP



Check



3/5VS load Switch
+5VALW To +5VS
+3VALW To +3VS

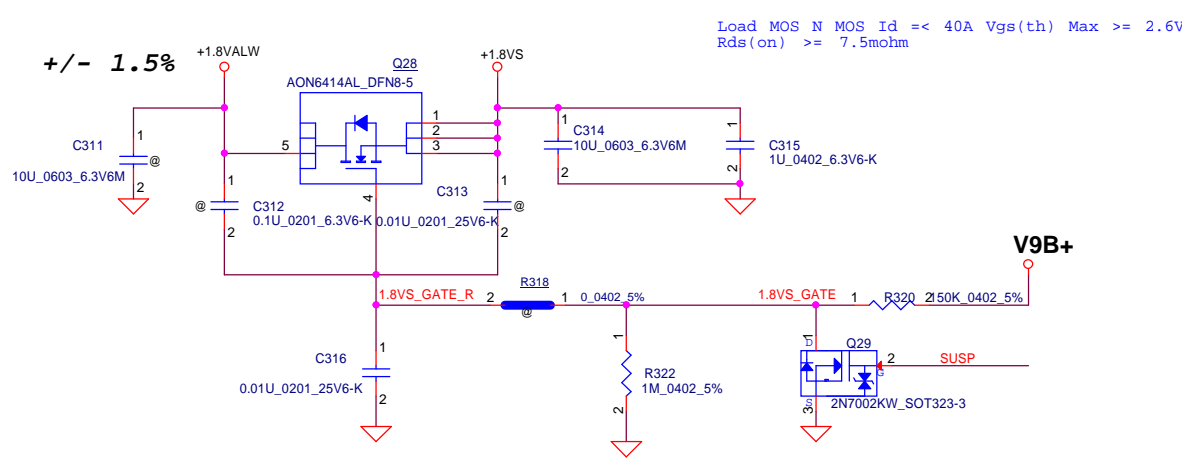
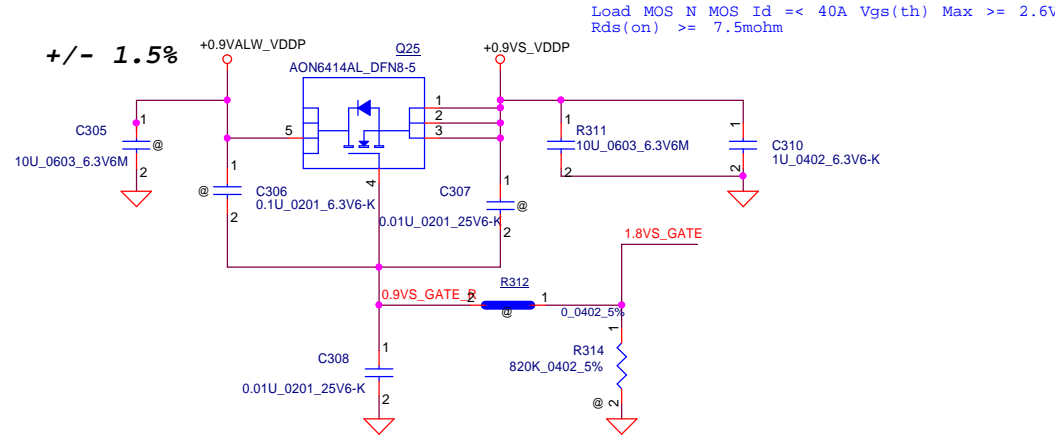


+0.9VALW_VDDP to +VDDP 10A request
V9B+ 9V--1.3V

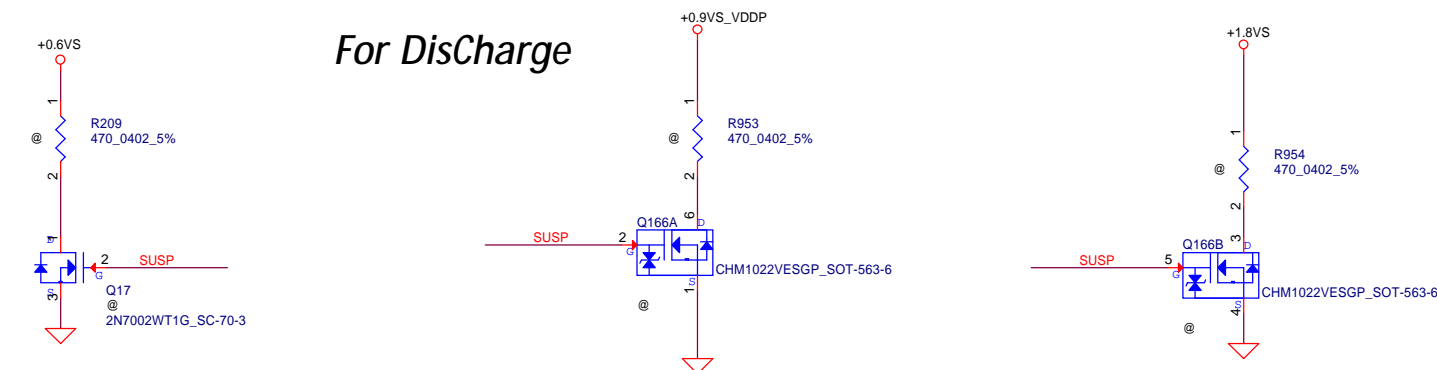
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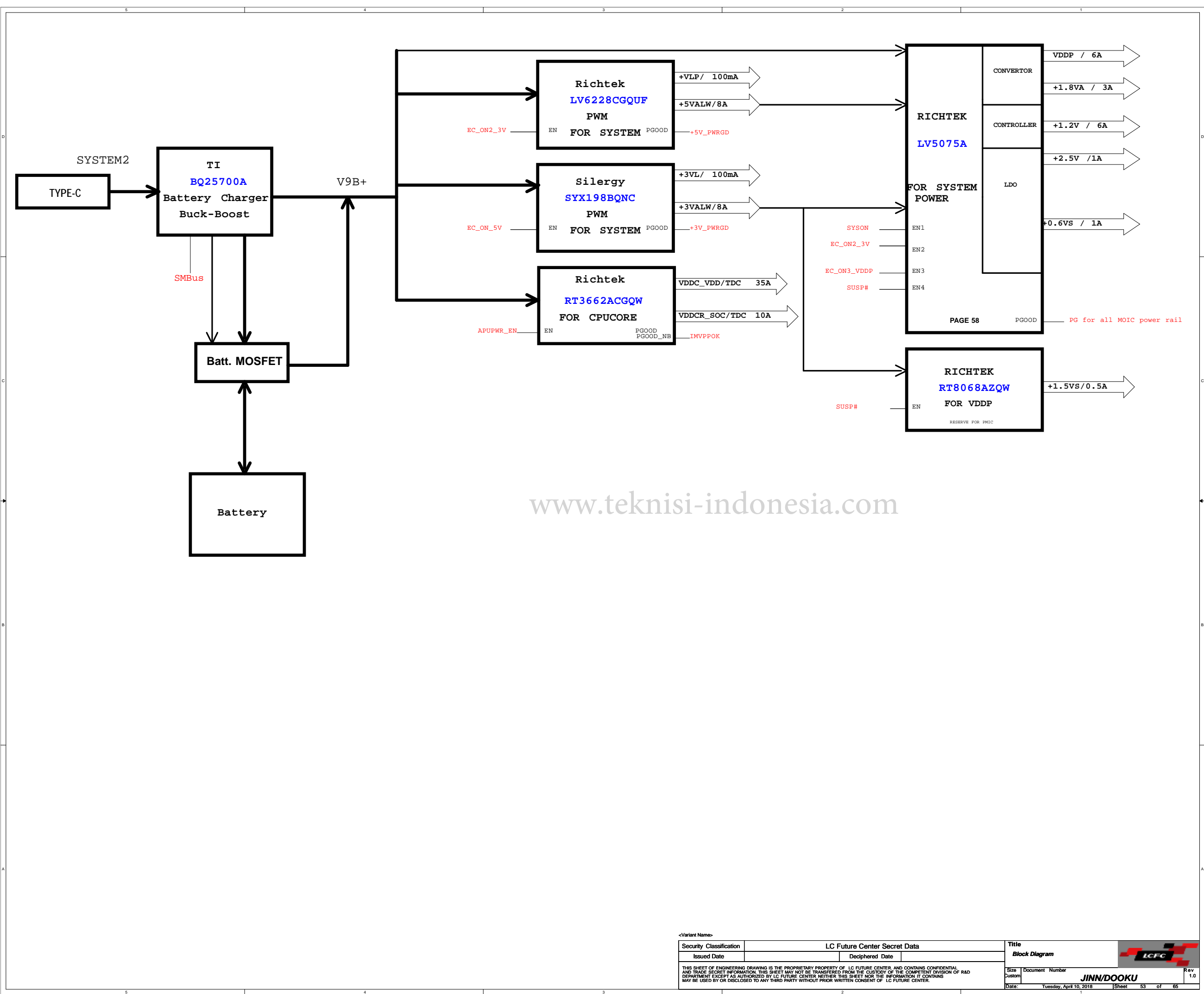
+1.8VALW to +1.8VS 2A request

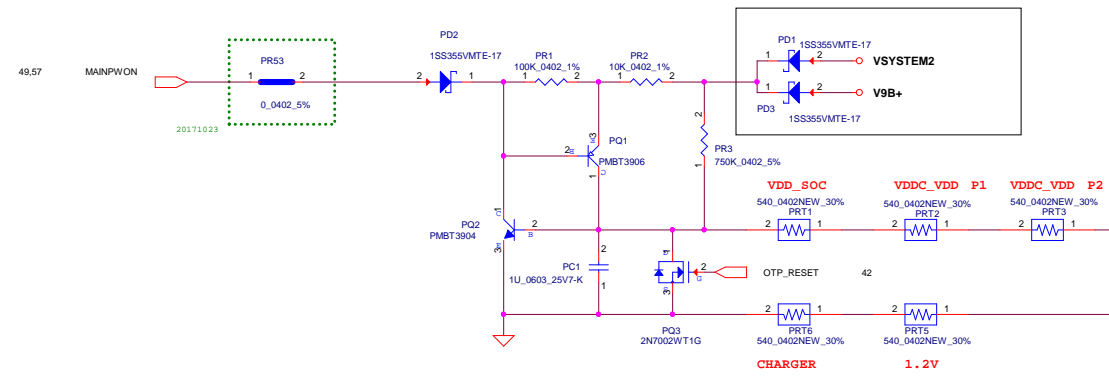


For DisCharge

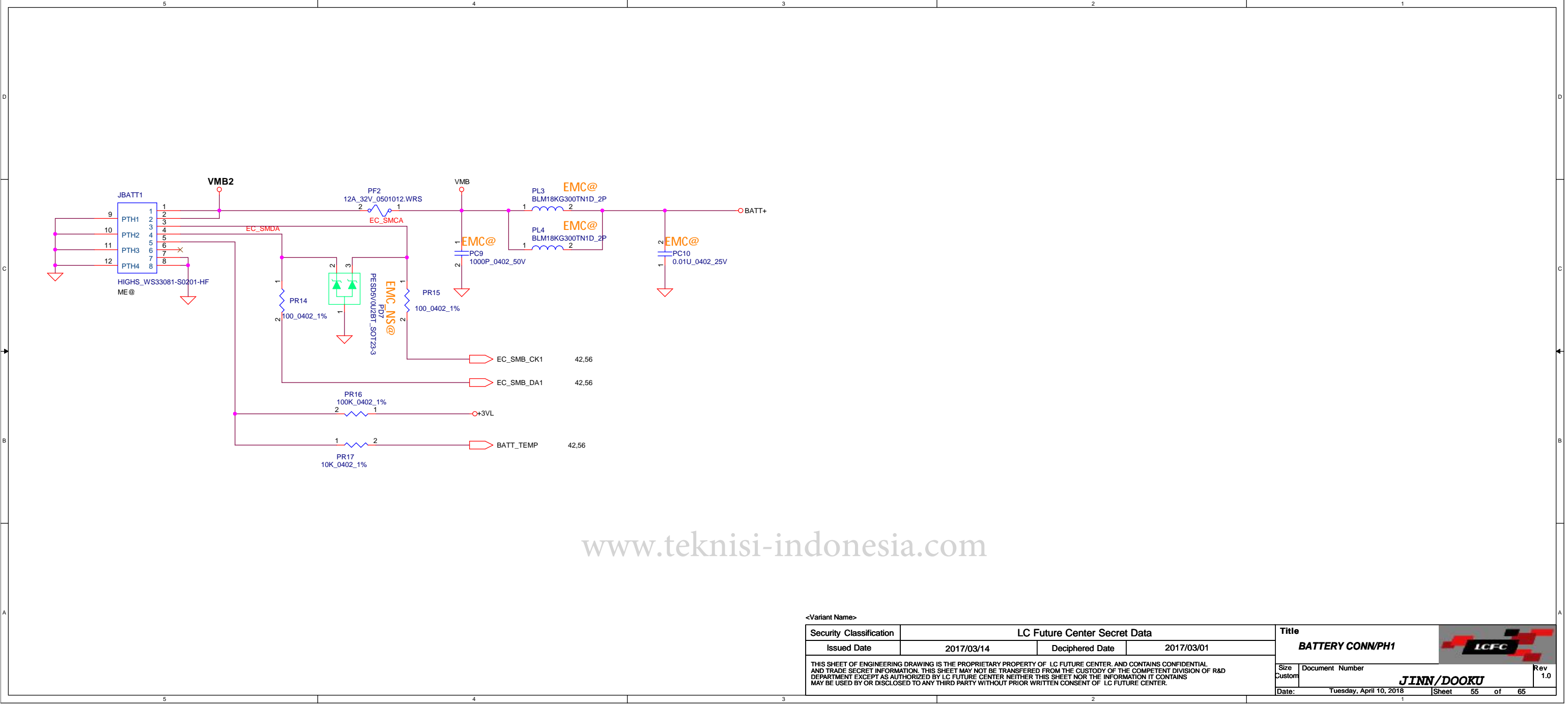


Security Classification	LC Future Center Secret Data			Title	3VS/5VS/1.1VS/VDDIO_RUN
Issued Date	2017/02/16	Deciphered Date	2018/06/01	Size	
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				JINN/DOOKU	1.0
Date: Tuesday, April 10, 2018				Sheet	51 of 65




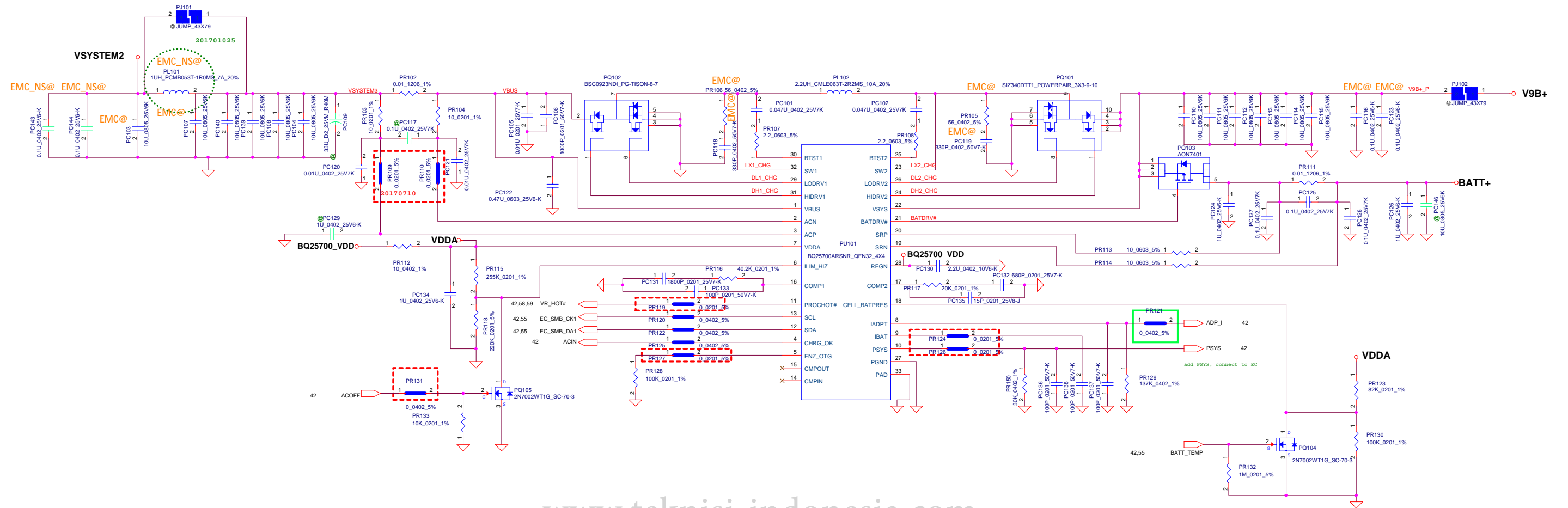


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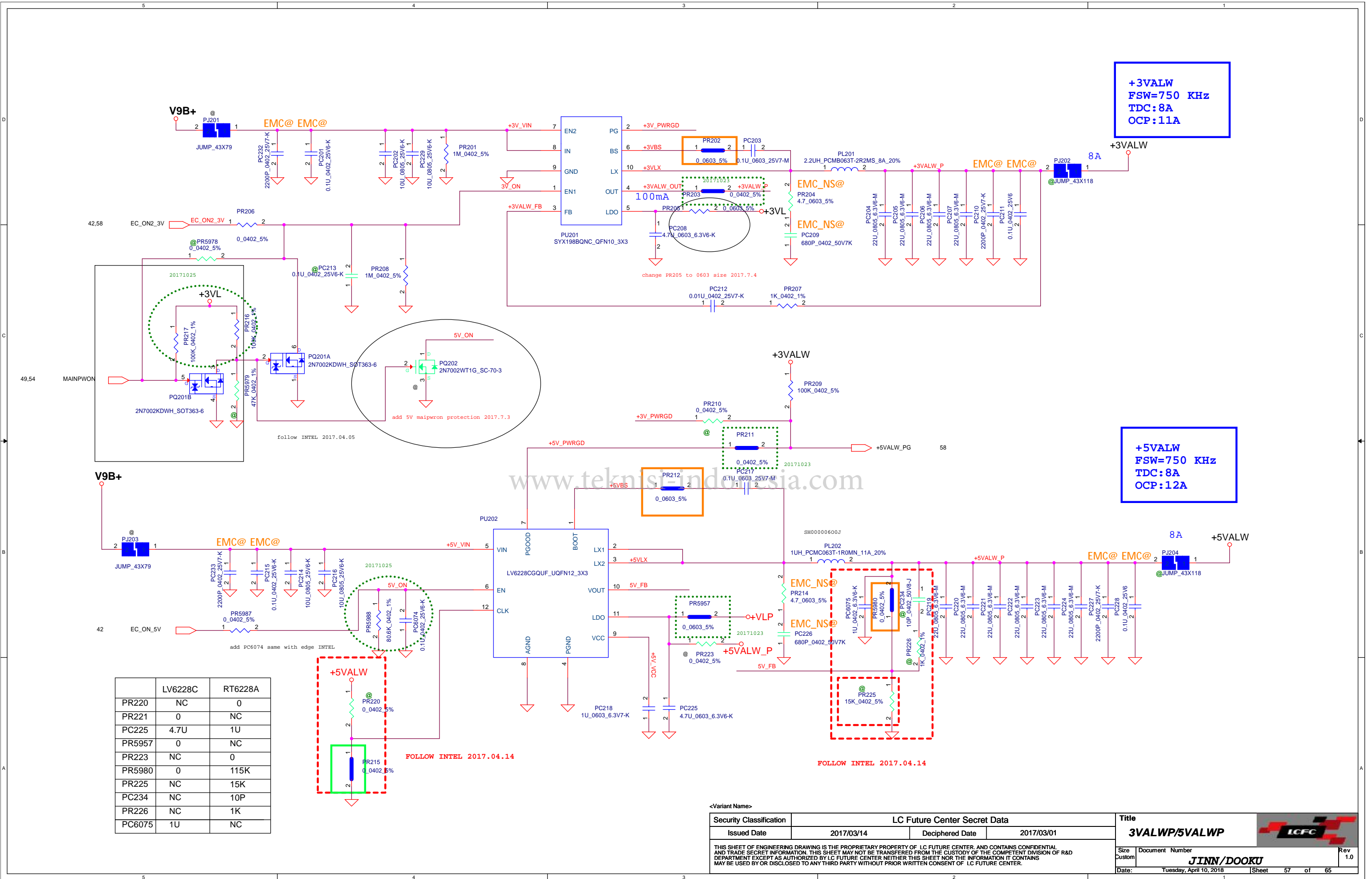
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Security Classification	LC Future Center Secret Data		
Issued Date	2017/03/14	Deciphered Date	2017/03/01
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BATTERY CONN/PH1		
Size Custom	Document Number	
JINN/DOOKU		Rev 1.0
Date:	Tuesday, April 10, 2018	Sheet 55 of 65



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Issued Date	2013/08/05	Deciphered Date	2014/12/31
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Size	Document	Number	Rev
Custom		EE480 NM-B421	1.0
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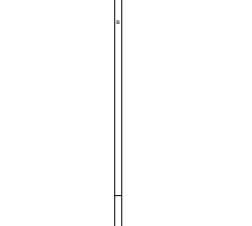
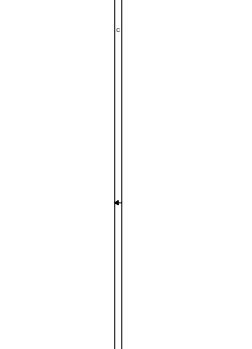
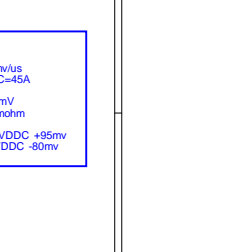
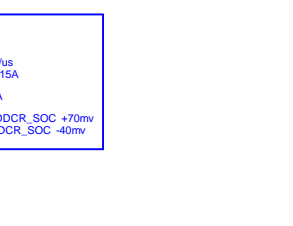
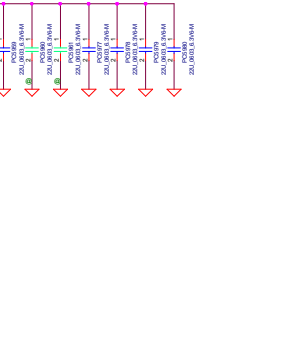
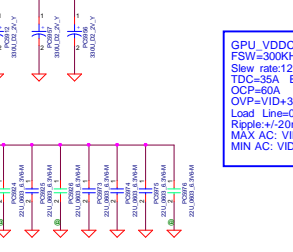
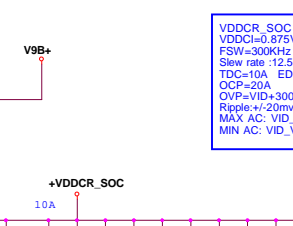
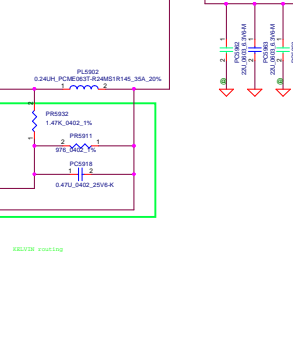
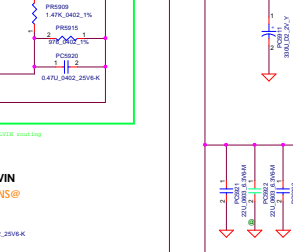
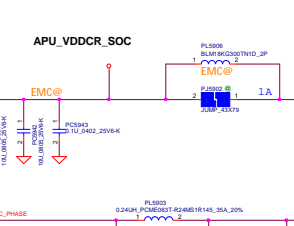
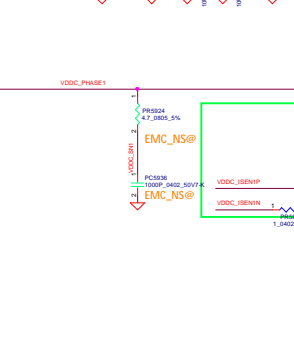
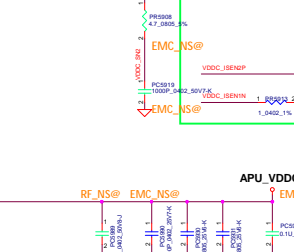
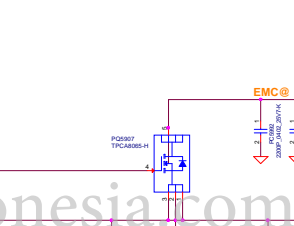
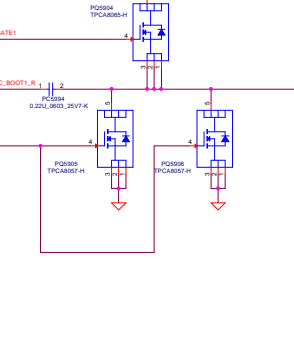
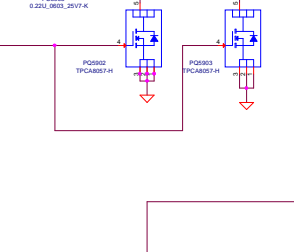
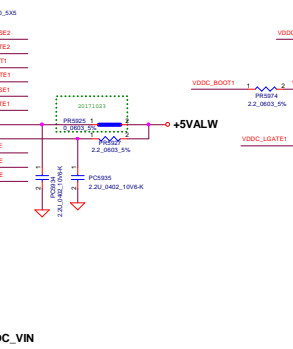
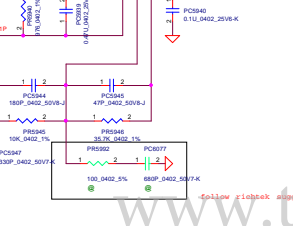
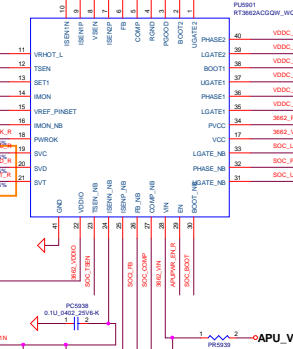
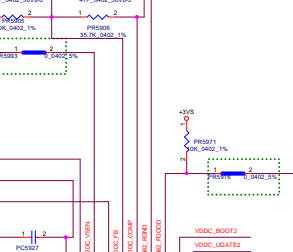
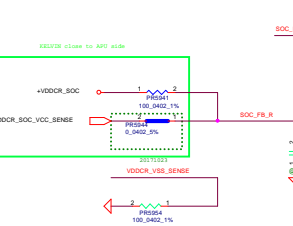
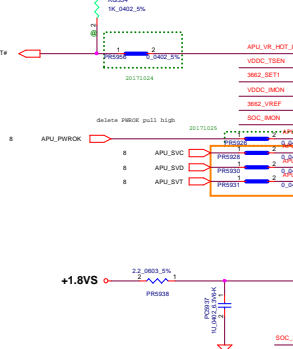
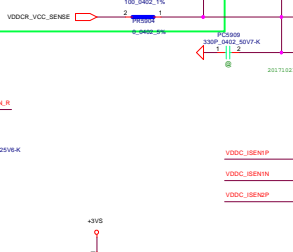
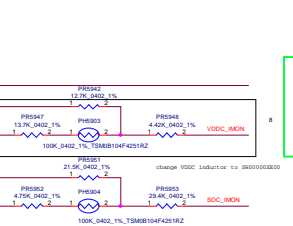
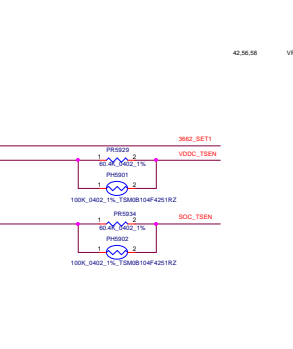
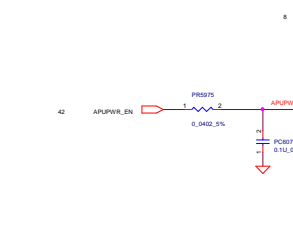
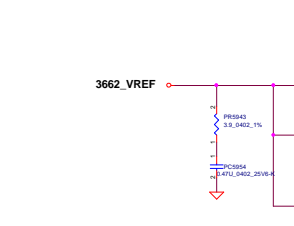
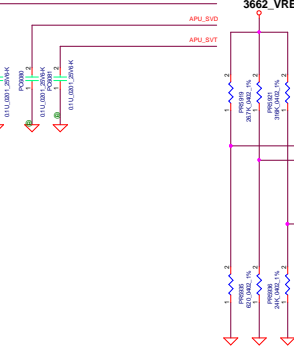
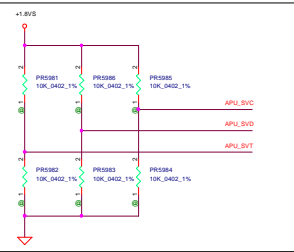


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PR226	NC	1K
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SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V



GPU_VDDC:
FSW=300KHz
Slew rate=12.5mV/us
TDC=35A EDC=45A
OCP=60A
OVP=VID+300mV
Load Line=0.6mohm
Ripple=+/-20mV
MAX AC: VID_VDDC +95mV
MIN AC: VID_VDDC -80mV

VDDCR_SOC
VDDC=0.975V
FSW=300KHz
Slew rate=12.5mV/us
TDC=10A EDC=15A
OCP=20A
OVP=VID+300mV
MAX AC: VID_VDDCR_SOC +70mV
MIN AC: VID_VDDCR_SOC -40mV

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Rev	1.0	Document Number	JINI/DOOKU		Rev 1.0
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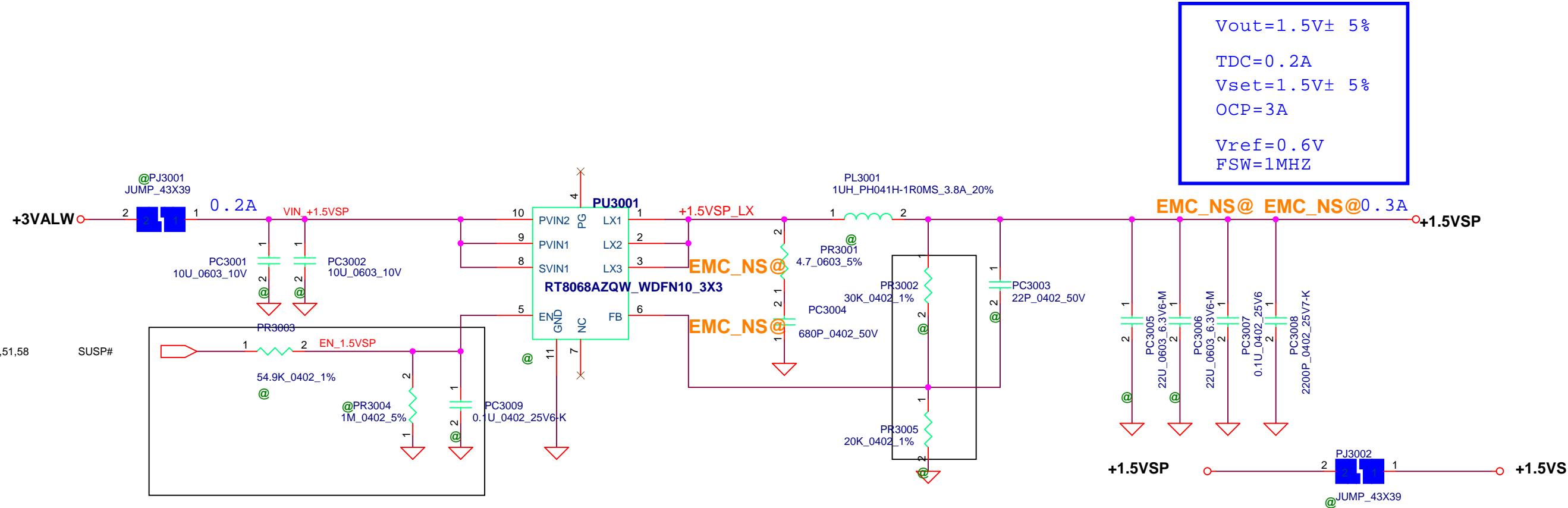
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Title		
+1.5VS		
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